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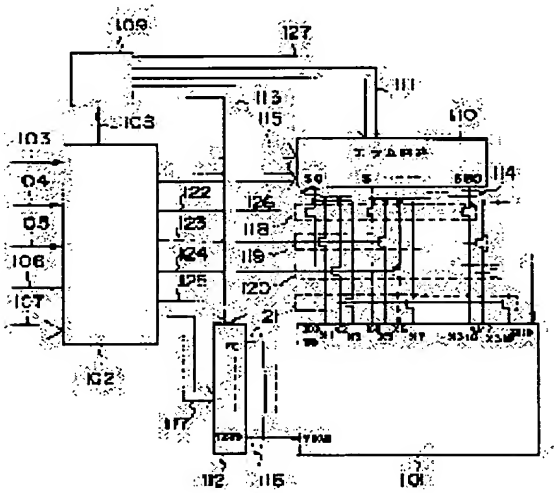
(54) LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PURPOSE: To realize a display controller for performing a satisfactory display to a liquid crystal panel in which a pixel pitch is made fine by using a conventional liquid crystal driving circuit.

CONSTITUTION: Display data are rearranged in accordance with switching groups 118 to 121 by a display controller 102. Then, display data are successively outputted to a column circuit 110 for every data corresponding to respective switching groups. Then, switching groups 118 to 121 are made to be opened and closed by control signals 122 to 125 in accordance with display data to be displayed. Consequently, the display data can be outputted only to X electrodes connected to the switching group to which pertinent display data are made to correspond. Thus, this controller can cope with a high difinition liquid crystal panel without necessitating the increasing of the number of output terminals of the column circuit and the fining of the pich of the output perminal.



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CLAIMS

[Claim(s)]
[Claim 1] The liquid crystal panel of the active-matrix mold equipped with M Y electrodes and X electrode of N individual, The selection electrical-potential-difference terminal which is equipped with the function which generates a selection electrical potential difference, a non-choosing electrical potential difference, and two or more kinds of gradation electrical potential differences, and outputs the above-mentioned selection electrical potential difference, The power circuit equipped with the non-choosing electrical-potential-difference terminal which outputs the above-mentioned non-choosing electrical potential difference, and the gradation electrical-potential-difference terminal which outputs the above-mentioned gradation electrical potential difference, The column circuit which is equipped with n output terminals (n<N), chooses for this every output terminal corresponding to the data stream which was able to give separately either of the above-mentioned gradation electrical potential differences outputted from the above-mentioned power circuit, and outputs the this chosen gradation electrical potential difference from the output terminal concerned, The above-mentioned selection electrical potential difference to any one of the above-mentioned Y electrodes Moreover, a common means to impress the above-mentioned non-choosing electrical potential difference to other Y electrodes, A component classifies the above-mentioned X electrode into two or more groups who are n or less pieces, and chooses any one of these groups. X electrode switching means connected with the correspondence relation to which only X electrode belonging to the this selected group was beforehand determined as the above-mentioned output terminal of the above-mentioned column circuit, The indicative data and the Horizontal Synchronizing signal are inputted from the outside at least. The liquid crystal display characterized by having the display controller outputted to the above-mentioned column circuit one by one for every assembly of the indicative data which corresponds mutually.
[Claim 2] The 1st memory the above-mentioned display controller can remember the data for at least one line to be, The 2nd memory which can memorize the data for at least one line, and the write-in means which takes in the indicative data inputted from the outside and is written in the 1st memory of the above, or the 2nd memory, From the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means among the 1st memory of the above, and the 2nd memory at the time A read-out means to begin to read the indicative data already stored in the memory concerned, and to output it one by one for every assembly of the indicative data which corresponds mutually, After the above-mentioned column circuit finishes outputting a gradation electrical potential difference to X electrode belonging to a certain group, selection of the above-mentioned group according to the above-mentioned X electrode switching means before starting the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- with the selection directions means made to change so that the next group's X electrode and the output terminal of a column circuit may be connected The liquid crystal display characterized by being constituted including the control means to which the memory made into the object of write-in actuation of the above-mentioned indicative data based on the above-mentioned write-in means is made to be changed by turns between the 1st memory of the above, and the 2nd memory of the above ignited by the above-mentioned Horizontal Synchronizing signal becoming effective.

[Claim 3] It is what is performed by the input from the outside of the above-mentioned indicative data being parallel in a liquid crystal display according to claim 1. Receive only several pixel minutes which was able to define beforehand the indicative data inputted from the above-mentioned outside, and this beam indicative data with a receptacle is classified based on the group to whom X electrode with which the indicative data concerned corresponds belongs. It is the liquid crystal display which is further equipped with a conversion means to output for this every classification, and is characterized by the above-mentioned write-in means being what writes the indicative data which the above-mentioned conversion means outputs in the 1st memory of the above, or the 2nd memory of the above.
[Claim 4] In a liquid crystal display according to claim 1 the above-mentioned write-in means It is what performs the above-mentioned write-in actuation synchronizing with the write-in clock generated separately. The above-mentioned read-out means The above-mentioned write-in clock is what performs the above-mentioned read-out synchronizing with the asynchronous read-out clock by which special generation is carried out. The above-mentioned control means The change of memory made into the write-in object of the above-mentioned indicative data based on the above-mentioned write-in means It is the liquid crystal display which checks having written in the indicative data for one screen, is made to perform it instead of the above-mentioned Horizontal Synchronizing signal, and is characterized by equipping the 1st memory of the above, and the 2nd memory of the above with the storage capacity which can memorize the indicative data for the liquid crystal panel 1 above-mentioned screen.
[Claim 5] In a liquid crystal display according to claim 1 the above-mentioned common means The common circuit which is equipped with m output terminals (m<M), makes sequential selection of one of these output terminals, and outputs a non-choosing electrical potential difference for the selection electrical potential difference above-mentioned [from the this chosen output terminal] from other output terminals, While connecting with the correspondence relation to which only Y electrode which divides the above-mentioned Y electrode into two or more groups whose components are m or less pieces, and belongs to one of groups was alternatively determined as the above-mentioned output terminal of the above-mentioned common circuit beforehand It has Y electrode switching means which connects to the non-choosing electrical-potential-difference terminal of the above-mentioned power circuit Y electrode which is not connected with the above-mentioned common circuit at the time. The above-mentioned display controller The liquid crystal display characterized by being the thing which makes selection of the above-mentioned group by the above-mentioned Y electrode switching means change every whenever the above-mentioned common circuit finishes choosing all output terminals.
[Claim 6] It is the liquid crystal display characterized by constituting the 1st memory of the above, and the 2nd memory of the above possible [modification of the storage capacity] in a liquid crystal display according to claim 1.
[Claim 7] The liquid crystal panel of the active-matrix mold equipped with M Y electrodes and X electrode of N individual, The column circuit which outputs the gradation electrical potential difference corresponding to the data stream which was equipped with n output terminals (n<N) and was separately given from this output terminal, A component classifies the above-mentioned X electrode into two or more groups who are n or less pieces, and chooses any one of these groups. X electrode switching means connected with the correspondence relation to which only X electrode belonging to the this selected group was beforehand determined as the above-mentioned output terminal of the above-mentioned column circuit, In the display controller used for the drive of the liquid crystal display which consisted of ****** The 1st memory which can memorize the data for at least one line, and the 2nd memory which can memorize the data for at least one line, The write-in means which takes in the indicative data inputted from the outside and is written in the 1st memory of the above, or the 2nd memory, From the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means among the 1st memory of the above, and the 2nd memory at the time A read-out means to begin to read the indicative data already stored in the memory concerned, and to output it one by one for every assembly of the indicative data which corresponds mutually, After

the above-mentioned column circuit finishes outputting a gradation electrical potential difference to X electrode belonging to a certain group, selection of the above-mentioned group according to the above-mentioned X electrode switching means before starting the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- with the selection directions means made to change so that the next group's X electrode and the output terminal of a column circuit may be connected It carries out an opportunity [the above-mentioned Horizontal Synchronizing signal becoming effective about the memory made into the object of write-in actuation of the above-mentioned indicative data based on the above-mentioned write-in means]. The display controller characterized by being constituted including the control means made to be changed by turns between the 1st memory of the above, and the 2nd memory of the above.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a suitable liquid crystal display controller to display indicative datas, such as a personal computer and a workstation, on a liquid crystal panel.
[0002]
[Description of the Prior Art] By the personal computer and workstation, the liquid crystal display is used widely.
[0003] Hereafter, the configuration and actuation of a liquid crystal display are explained using drawings 1717 , 18, and 19. Horizontal resolution gives explanation here taking the case of the case where the liquid crystal panel 640 pixels per each pixel of R, G, and B (a total of 1920 (= 640x3) pixels) and whose vertical definition are 480 lines is driven by the display controller (trade name" column circuit HD66310") by Hitachi, Ltd. in addition -- the contents of this explanation -- the Hitachi LCD driver LSI data book p of the Hitachi, Ltd. semi-conductor operation division issue -- it is indicated by 661 and 662.
[0004] The indicative data 2401 and the synchronizing signal 2402 which synchronized with this are inputted into the driver control means 2110 from the personal computer, the workstation, etc. as shown in drawing 17 . In addition, a dot clock, a Horizontal Synchronizing signal, and a Vertical Synchronizing signal are included in a synchronizing signal 2402.
[0005] The data-conversion circuit 2120 within the driver control means 2110 has changed the indicative data 2401 so that it may double with the interface of the column circuit 2100 mentioned later. And the data after this conversion are outputted as an indicative data 2103 for drivers (refer to drawing 18).
[0006] A frequency divider 2121 is carrying out dividing of the dot clock contained in the synchronizing

signal 2402, and an indicative data generates the indicative-data incorporation clock 2111 during an effective period, and it is outputting this (refer to drawing 18).
[0007] Moreover, a delay circuit 2122 delays the Horizontal Synchronizing signal included in the synchronizing signal 2402, and is generating and outputting the indicative-data latch clock 2104 and the enable signal 2105 (refer to drawing 18).
[0008] The indicative data 2103 for drivers and the indicative-data incorporation clock 2111 are outputted to the column circuit 2100 among these signals. On the other hand, the enable signal 2105 is outputted to the scan drive circuit 2131. Indicative-data latch KURO@KKU 2104 is outputted to both the column circuit 2100 and the scan drive circuit 2131.
[0009] The column circuit 2100 incorporates the indicative data 2103 for drivers in falling of the indicative-data incorporation clock 2111. Here, since the column circuit HD 66310 by Hitachi, Ltd. currently used as a column circuit 2100 is what has a-160 output, it is carrying out 12-piece (= 1920/160) use of HD66310 in this liquid crystal display. Hereafter, the column circuit 2100-1 to 2100-12 is generically called the column circuit group 2130. The column circuit 2100 incorporates the indicative data 2103 for drivers, only when the enable signal input EIO1 is a low level.
[0010] Moreover, if this column circuit 2100 incorporates the indicative data for 60 pixels, the enable signal output EIO2 will change from high level to a low level. And the enabling output signal EIO2 of the column circuit 2100 located in left-hand at the enable signal input EIO1 of each column circuit 2100 is inputted. In addition, the enable signal input EIO1 is grounded about the column circuit 2100-1 located in a high-order end. In addition, the back explains the internal configuration of the column circuit HD 66310 more concretely.
[0011] If the column circuit 2100-1 completes incorporation for the indicative data 2103 for 160 pixels, the enabling output signal EIO2 will change from high level to a low level. Then, the column circuit 2100-2 of the next step (right-hand) is enabling. And the column circuit 2100-2 concerned starts incorporation of an indicative data 2103 shortly.
[0012] It incorporates 160 pixels of indicative datas at a time one by one from the column circuit 2100 located in left-hand side similarly hereafter.
[0013] And if it finishes incorporating the indicative data 2103 for drivers for one line, the column Cairo group 2130 will impress the display electrical potential difference corresponding to the indicative data concerned for one line to a liquid crystal panel 2132.
[0014] On the other hand, the scan drive circuit 2131 is scanning vertical lines sequentially synchronizing with an enable signal 2105.
[0015] The indicative data (data which the latch circuit 2303 mentioned later latches) which the column circuit 2100 outputs will be then displayed in Rhine chosen by the scan drive circuit 2131.
[0016] In addition, the writing of data is performed even when an indicative data does not change for every Rhine.
[0017] Next, the outline of the column circuit HD 66310 is explained using drawing 19 .
[0018] It has the composition that this input indicative data 2103 for 4 pixels is parallel, and is inputted in the column circuit HD 66310. The input indicative data 2103 is a gradient data triplet about each pixel. Moreover, it has 160 signal lines 2101 for outputting liquid crystal driver voltage.
[0019] The latch address counter 2301 counts falling of the indicative-data incorporation clock 2111, and generates a latch signal. In addition, the indicative-data incorporation clock 2111 has come to be able to carry out a mask in the enable signal input EIO1. A latch signal is not generated when the enable signal input EIO1 is high-level. Moreover, after counting the indicative-data incorporation clock 2111 40 times, the enable signal output EIO2 is made into a low level. In addition, since the indicative data for 4 pixels can be incorporated at once as mentioned later, 40 counts are equivalent to incorporation of the indicative data for 160 (= 4x40) pixels.
[0020] The latch circuit 2302 is divided into every 4-pixel 40 steps. This latch circuit 2302 incorporates the indicative data 21003 for drivers by 4 pixels to coincidence synchronizing with the latch signal from

the latch address counter 2301.
[0021] The latch circuit 2303 consists of latch circuits for 160 pixels. A latch circuit 2303 latches the indicative data which the latch circuit 2302 incorporated synchronizing with the indicative-data latch clock 2104. And one-line time amount maintenance of this latched data is carried out.
[0022] The level-shifter circuit 2304 decodes the indicative data which the latch circuit 2303 latched, and generates the select signal for choosing liquid crystal applied voltage.
[0023] The liquid crystal drive circuit 2305 chooses one of the liquid crystal driver voltages 2306 whose eight kinds exist according to a select signal, and outputs it to X electrode of a liquid crystal panel by making the this chosen electrical potential difference into applied voltage 2101.
[0024] As stated above, the display action in a liquid crystal display is the repeat of the most latch actuation of the indicative data to the column circuit 2100.
[0025] In addition to this, the horizontal direction of a liquid crystal panel is divided into two fields, and there is a thing of transmitting the indicative data for every field to coincidence in the drive method of a liquid crystal display. in this drive method, while it has two display memory and the indicative data is written in one side, an indicative data is read from the display memory of another side, and it is this reading **** -- the indicative data is outputted to parallel. Such a technique is indicated by JP,1-113793,A, JP,2-126285,A, and JP,5-232898,A, for example.
[0026]
[Problem(s) to be Solved by the Invention] A liquid crystal panel is also asked for a highly minute display in current. In order to correspond to this, not only detailed-izing of a pixel pitch but the output pitch of a column circuit must be made detailed. This is because cascade connection which the column circuit mentioned above cannot be performed. Moreover, formation of small area of the column circuit itself, small pitch-ization of TAB which makes liquid crystal panel connection of the output of a column circuit, etc. must be attained.
[0027] However, when TAB and a liquid crystal panel were made detailed, the alignment and the junction technique for the joint will take an advanced technique, and another problem that a production cost became high was produced. Therefore, the technique corresponding to the liquid crystal panel of a highly minute display was searched for, using the conventional liquid crystal drive circuit.
[0028] It aims at offering the display controller which can respond to the liquid crystal panel which made the pixel pitch detailed, the conventional liquid crystal drive circuit being used for this invention.
[0029]
[Means for Solving the Problem] This invention is what was made in order to attain the above-mentioned purpose. As the 1st mode The liquid crystal panel of the active-matrix mold equipped with M Y electrodes and X electrode of N individual, The selection electrical-potential-difference terminal which is equipped with the function which generates a selection electrical potential difference, a non-choosing electrical potential difference, and two or more kinds of gradation electrical potential differences, and outputs the above-mentioned selection electrical potential difference, The power circuit equipped with the non-choosing electrical-potential-difference terminal which outputs the above-mentioned non-choosing electrical potential difference, and the gradation electrical-potential-difference terminal which outputs the above-mentioned gradation electrical potential difference, The column circuit which is equipped with n output terminals ($n<N$), chooses for this every output terminal corresponding to the data stream which was able to give separately either of the above-mentioned gradation electrical potential differences outputted from the above-mentioned power circuit, and outputs the this chosen gradation electrical potential difference from the output terminal concerned, The above-mentioned selection electrical potential difference to any one of the above-mentioned Y electrodes Moreover, a common means to impress the above-mentioned non-choosing electrical potential difference to other Y electrodes, A component classifies the above-mentioned X electrode into two or more groups who are n or less pieces, and chooses any one of these groups. X electrode switching means connected with the correspondence relation to which only X electrode belonging to the this selected group was beforehand

determined as the above-mentioned output terminal of the above-mentioned column circuit, The indicative data and the Horizontal Synchronizing signal are inputted from the outside at least. The liquid crystal display characterized by having the display controller outputted to the above-mentioned column circuit one by one for every assembly of the indicative data which corresponds mutually is offered.
[0030] The 1st memory the above-mentioned display controller can remember the data for at least one line to be, The 2nd memory which can memorize the data for at least one line, and the write-in means which takes in the indicative data inputted from the outside and is written in the 1st memory of the above, or the 2nd memory, From the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means among the 1st memory of the above, and the 2nd memory at the time A read-out means to begin to read the indicative data already stored in the memory concerned, and to output it one by one for every assembly of the indicative data which corresponds mutually, After the above-mentioned column circuit finishes outputting a gradation electrical potential difference to X electrode belonging to a certain group, selection of the above-mentioned group according to the above-mentioned X electrode switching means before starting the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- with the selection directions means made to change so that the next group's X electrode and the output terminal of a column circuit may be connected It may be constituted including the control means to which the memory made into the object of write-in actuation of the above-mentioned indicative data based on the above-mentioned write-in means is made to be changed by turns between the 1st memory of the above, and the 2nd memory of the above ignited by the above-mentioned Horizontal Synchronizing signal becoming effective.
[0031] It is what is performed by the input from the outside of the above-mentioned indicative data being parallel. Receive only several pixel minutes which was able to define beforehand the indicative data inputted from the above-mentioned outside, and this beam indicative data with a receptacle is classified based on the group to whom X electrode with which the indicative data concerned corresponds belongs. It may have further a conversion means to output for this every classification, and the above-mentioned write-in means may write the indicative data which the above-mentioned conversion means outputs in the 1st memory of the above, or the 2nd memory of the above.
[0032] The above-mentioned write-in means is what performs the above-mentioned write-in actuation synchronizing with the write-in clock generated separately. The above-mentioned read-out means The above-mentioned write-in clock is what performs the above-mentioned read-out synchronizing with the asynchronous read-out clock by which special generation is carried out. The above-mentioned control means The change of memory made into the write-in object of the above-mentioned indicative data based on the above-mentioned write-in means It may check having written in the indicative data for one screen, it may be made to perform instead of the above-mentioned Horizontal Synchronizing signal, and the 1st memory of the above and the 2nd memory of the above may be equipped with the storage capacity which can memorize the indicative data for the liquid crystal panel 1 above-mentioned screen.
[0033] The common circuit which the above-mentioned common means is equipped with m output terminals (m<M), makes sequential selection of one of these output terminals, and outputs a non-choosing electrical potential difference for the selection electrical potential difference above-mentioned [from the this chosen output terminal] from other output terminals, While connecting with the correspondence relation to which only Y electrode which divides the above-mentioned Y electrode into two or more groups whose components are m or less pieces, and belongs to one of groups was alternatively determined as the above-mentioned output terminal of the above-mentioned common circuit beforehand It has Y electrode switching means which connects to the non-choosing electrical-potential-difference terminal of the above-mentioned power circuit Y electrode which is not connected with the above-mentioned common circuit at the time. The above-mentioned display controller it is the thing which makes selection of the above-mentioned group by the above-mentioned Y electrode switching means change every whenever the above-mentioned common circuit finishes choosing all

output terminals -- it is desirable.
[0034] As for the 1st memory of the above, and the 2nd memory of the above, being constituted possible [modification of the storage capacity] is more desirable.
[0035] The liquid crystal panel of the active-matrix mold equipped with M Y electrodes and X electrode of N individual as the 2nd mode of this invention, The column circuit which outputs the gradation electrical potential difference corresponding to the data stream which was equipped with n output terminals (n<N) and was separately given from this output terminal, A component classifies the above-mentioned X electrode into two or more groups who are n or less pieces, and chooses any one of these groups. X electrode switching means connected with the correspondence relation to which only X electrode belonging to the this selected group was beforehand determined as the above-mentioned output terminal of the above-mentioned column circuit, In the display controller used for the drive of the liquid crystal display which consisted of ****** The 1st memory which can memorize the data for at least one line, and the 2nd memory which can memorize the data for at least one line, The write-in means which takes in the indicative data inputted from the outside and is written in the 1st memory of the above, or the 2nd memory, From the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means among the 1st memory of the above, and the 2nd memory at the time A read-out means to begin to read the indicative data already stored in the memory concerned, and to output it one by one for every assembly of the indicative data which corresponds mutually, After the above-mentioned column circuit finishes outputting a gradation electrical potential difference to X electrode belonging to a certain group, selection of the above-mentioned group according to the above-mentioned X electrode switching means before starting the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- with the selection directions means made to change so that the next group's X electrode and the output terminal of a column circuit may be connected It carries out an opportunity [the above-mentioned Horizontal Synchronizing signal becoming effective about the memory made into the object of write-in actuation of the above-mentioned indicative data based on the above-mentioned write-in means]. The display controller characterized by being constituted including the control means made to be changed by turns between the 1st memory of the above and the 2nd memory of the above is offered.
[0036]
[Function] The power circuit is outputting [the selection electrical potential difference from a selection electrical-potential-difference terminal] the gradation electrical-potential-difference terminal from a gradation electrical-potential-difference terminal for the non-choosing electrical potential difference from the non-choosing electrical-potential-difference terminal.
[0037] X electrode switching means classified the above-mentioned X electrode into two or more groups who are n or less pieces, and the component has connected it with the correspondence relation to which only X electrode which chooses any one of these groups and belongs to the this chosen group was beforehand determined as the above-mentioned output terminal of the above-mentioned column circuit.
[0038] A display controller is outputted to the above-mentioned column circuit one by one for every assembly of the indicative data which corresponds mutually. A display controller can be constituted as follows, for example.
[0039] A write-in means takes in the indicative data inputted from the outside, and is writing it in the 1st memory of the above, or the 2nd memory. Among the 1st memory and the 2nd memory, at the time, a read-out means is beginning to read the indicative data already stored in the memory concerned one by one for every assembly of the indicative data which corresponds mutually, and is outputting it from the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means. The control means is making the memory made into the object of write-in actuation of the indicative data based on a write-in means changed by turns between the 1st memory of the above, and the 2nd memory of the above ignited by a Horizontal Synchronizing signal becoming

effective at this time. Thereby, by turns, writing/read-out of every one line are performed in the 1st memory and 2nd memory, and an indicative data goes to them. It writes in or rearrangement is performed by specifying this address corresponding to each group, and going in the case of read-out.
[0040] A column circuit outputs the gradation electrical potential difference which chose and this chose either of the gradation electrical potential differences for every output terminal corresponding to the data stream to which it is given from a display controller from the output terminal concerned. selection of the group according to X electrode switching means after finishing outputting a gradation electrical potential difference to X electrode with which a column circuit belongs to a certain group at this time, before the selection directions means of a display controller starts the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- it is made to change so that the next group's X electrode and the output terminal of a column circuit may be connected Consequently, the gradation electrical potential difference which is outputting the column circuit then will be impressed to X electrode belonging to the group chosen at this time.
[0041] In addition, when parallel, an indicative data is classified for every group according to a conversion means, and it is made for the input from the outside of an indicative data to make it output for this every classification with it. And a write-in means should just write the indicative data which a conversion means outputs in the 1st memory of the above, or the 2nd memory of the above. moreover, the clock with which a write-in means synchronizes and the clock with which a read-out means synchronizes -- mutual -- asynchronous ** -- in a certain case, a control means checks having written in the indicative data for one screen for the change of memory made into the write-in object of the above-mentioned indicative data based on the above-mentioned write-in means, and is made to carry it out to it. And the 1st memory and 2nd memory of the above are equipped with the storage capacity which can memorize the indicative data for the liquid crystal panel 1 above-mentioned screen.
[0042] On the other hand, a common means impresses the above-mentioned non-choosing electrical potential difference to other Y electrodes for a selection electrical potential difference again any one of the Y electrodes. This common means can be constituted as follows, for example. A common circuit makes sequential selection of one of these output terminals, and is outputting the non-choosing electrical potential difference for the selection electrical potential difference above-mentioned [from the this chosen output terminal] from other output terminals. Y electrode switching means divides Y electrode into two or more groups whose components are m or less pieces, and connects it with the correspondence relation to which only Y electrode belonging to one of groups was alternatively determined as the above-mentioned output terminal of the above-mentioned common circuit beforehand. Moreover, Y electrode which is not connected with the above-mentioned common circuit at the time is connected to the non-choosing electrical-potential-difference terminal of the above-mentioned power circuit. And a display controller makes the selection situation by the above-mentioned Y electrode switching means change every, whenever a common circuit finishes choosing all output terminals.
[0043]
[Example] The example of this invention is explained using a drawing.
[0044] The 1st example of this invention is explained using drawing 6 from drawing 1 .
[0045] the column circuit 110 for driving X electrode of a liquid crystal panel 101 and a liquid crystal panel 101 as the liquid crystal display of this example is shown in drawing 1 , the common circuit 112 for driving Y electrode of a liquid crystal panel 101, the display controller 102 that operates the column circuit 1110 and the common circuit 112 according to various signals, an indicative data, etc. which are inputted from the outside, and a power circuit 109 -- since -- it is constituted. Naturally, these are connected by the signal lines 103, 104, 105, 106,108,127,122-125 for delivering and receiving various signals etc., and buses 111, 113, and 115,126,117,107. Furthermore, in this example, connection between a liquid crystal panel 101 and the column circuit 110 is made through the switch groups 118-121 which operate according to the directions from the display controller 102. This example is characterized

[greatest] by to have formed these switch groups 118-121 and the display control corresponding to this.

[0046] In addition, since correspondence relation between an explanatory note and a drawing is made intelligible in the following explanation, the number of the signal line concerned and a bus may be attached and the signal delivered and received through these signal lines or a bus may be called. For example, suppose that the indicative data inputted through a bus 107 is called an indicative data 107. The same is said of explanation of other examples.

[0047] A liquid crystal panel 101 is the thing of the active-matrix mold which constitutes a matrix from 320 X electrodes and 240 Y electrodes, and has a switching element at the intersection.

[0048] The display controller 102 generates the indicative data 126 and the various signals for displaying on a liquid crystal panel 101 based on the indicative data 107 and the various control signals which are inputted from the outside. There are Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105 that shows the scope of an indicative data, and a dot clock 106 in the control signal inputted from the outside. An indicative data 107 synchronizes with a dot clock 106, it is the sequence according to the display position on a screen, and is serial and is sent.

[0049] The display controller 102 is generating and outputting the alternating current-ized signal 108, the column control signal 115, the common control signal 117, an indicative data 126, and the switch control signals 122-125 that control the switch groups 118-121 based on these control signals 103-106 and an indicative data 107.

[0050] The display controller 102 of this example rearranged this indicative data 107 corresponding to the connection relation between the switch group 118 - 121 grades, and is equipped with the function outputted as an indicative data 126. In this example, after rearranging an indicative data corresponding to there being four switch groups, it is dividing and outputting to four groups. This group division is performed by classifying the display position on a screen according to the system of residues of 4. This responds to the connection relation between each switch groups 118-121 and X electrode following the system of residues of 4. Within each group, a display position is more previously outputted by the thing in left-hand side. The detail of this display controller 102 and this rearrangement is explained a back forge fire.

[0051] A power circuit 109 is for generating the various electrical potential differences (the counterelectrode electrical potential difference 127, the gradation electrical potential difference 111, selection / non-choosing electrical potential difference 113) impressed to a liquid crystal panel. The gradation electrical potential difference 111 is generated synchronizing with the alternating current-ized signal 108, and is supplied to the column circuit 110. There are a thing of straight polarity and a thing of negative polarity in this gradation electrical potential difference 111 to the counterelectrode electrical potential difference 127. Selection / non-choosing electrical potential difference 113 is outputted to the common circuit 112.

[0052] The column circuit 110 chooses either for every pixel among the gradation electrical potential differences inputted through the bus 111, and outputs what was this chosen from the output bus 114 (output terminals s0-s80). This gradation electrical potential difference is then supplied only to predetermined X electrode made into the output bus 114 and switch-on by switch 118 above-mentioned groups 118-121. This column circuit 110 is having the operating state controlled by the column circuit control signal 115 which the display controller 102 outputs.

[0053] The common circuit 112 outputs the selection electrical potential difference / non-choosing electrical potential difference inputted through a bus 113 to Y electrode of a liquid crystal panel 101 through the output bus 116. This common circuit 112 is having the operating state controlled by the common circuit control signal 117 which the display controller 102 outputs.

[0054] The switch groups 118-121 are for changing suitably the connection relation between the output terminals s0-s80 which constitute the output bus 114 of the column circuit 110, and X electrode (electrodes x0-x319) of a liquid crystal panel 101. Each switch groups 118-121 consist of 80 switches,

respectively. The electrodes x0-x319 of a liquid crystal panel 101 are divided into four groups by classifying the location from left-hand side according to the regulation (this example 4 system of residueses) which was able to be defined beforehand. The switch groups 118-121 connect only X electrode belonging to one of groups with the output bus 114 of a column circuit suitably by changing an ON/OFF condition according to the directions from control signals 122-125, respectively. Here, the switch belonging to the 1st switch group 118 is called a switch 1-1, a switch 1-2, --, a switch 1-80 sequentially from left-hand side. The switch belonging to the 2nd switch group is called a switch 2-1, a switch 2-2, --, a switch 2-80. The concrete ****** relation of the output terminals s0-s80 which adopt the way of calling with the same said of the switch belonging to the 3rd switch group 120 and the 4th switch group 121, the switch groups 181-121, and electrodes x0-x319 and ** is as follows. The output terminal s0 is connectable with an electrode x3 by the switch 4-1 with electrode x2 with an electrode x1 and a switch 3-1 by the electrode x0 and the switch 2-1 by the switch 1-1. Similarly, electrodes x4, x5, x6, and x7 and connection are possible for an output terminal s1 by the switch 1-2, 2-2, 3-2, and 4-2. Between output terminals s2-s80 and electrodes x8-x319 is connected with the same relation.

[0055] Therefore, the gradation electrical potential difference outputted from output terminals s0-s80 can be impressed to electrodes x0, x4, x8, x12, --, x316 by turning ON only the 1st switch group 118 (switch 1-1 to 1-80), and turning OFF other switch groups 119,120,121. If only the 2nd switch group 119 (switch 2-1 to 2-80) is turned ON, the gradation electrical potential difference similarly outputted from output terminals s0-s80 can be impressed to electrodes x1, x5, x9, x113, --, x317. The same is said of the 3rd switch group 120 (switch 3-1 to 3-80), and the 4th switch group 121 (switch 4-4 to 3-80).

[0056] The condition (ON/OFF) of the 1st switch group 118 is changed by the 1st control signal 122 which the display controller 102 outputs. The condition (ON/OFF) of the 2nd switch group 119 is changed by the 2nd control signal 123. The condition (ON/OFF) of the 3rd switch group 120 is changed by the 3rd control signal 124. The condition (ON/OFF) of the 4th switch group 121 has composition changed by the 4th control signal 125.

[0057] Next, the display controller 102 is further explained to a detail using drawing 2 . The display controller 102 is constituted including the clock control section 201, the memory system control bus 202, the memory control section 203, the memory control bus 204, the memory control bus 205, the bus control line 206, memory 207, memory 208, the data bus 209,210, the bus selector 211, and the latch circuit 213.

[0058] The clock control section 201 generates the alternating current-ized signal 108, the column control signal 115, the common control signal 117, and the switch control signals 122-125 based on Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105, and a dot clock 106. Furthermore, the clock control section 201 is also generating the memory system control signal 202 and the latch clock 214 which control the inside of the display controller 102.

[0059] The memory system control signal 202 is constituted including the read-out clock. The latch clock 214 synchronizes with the data transfer clock in the column control bus 115. Moreover, the data transfer clock in below-mentioned drawing 4 and drawing 6 and the output clock are contained in the column control signal 115. Moreover, FLM in drawing 6 and the Rhine signal are included in the common control signal 117.

[0060] The memory control sections 203 are the writing of the data to memory 207,208 / thing for reading and controlling the condition of the bus selector 211. Therefore, the memory control section 203 generates the memory control signal 204,205 which synchronized with the memory system control signal 202, and is outputting it to each memory 207,208. The write enable signal in drawing 3 which makes memory 207,208 the condition which can be written in, and the lead enable signal made into the condition which can be read and the address signal which writes in data and specifies the address are contained in the memory control signal 204,205.

[0061] Furthermore, the memory control section 203 is outputting the bus control signal 206 to the bus selector 211. The memory control section 203 makes the bus control signal 206 a "low", when

performing the writing to memory 207, performing the bus control signal 206 to "yes" and writing in memory 208 on the other hand.
[0062] Memory 207 and memory 208 have the storage capacity which can memorize the indicative data for one line, respectively. The writing of the data to this memory 207 and 208 and read-out are made through a data bus 209 and a data bus 210.
[0063] Rearrangement of an above-mentioned indicative data has composition performed in connection with storing of the indicative data to this memory 207 (or 208), and read-out.
[0064] The bus selector 211 is for choosing either of the memory 207,208 and writing in an indicative data 107. Moreover, either memory 207 or the memory 208 is chosen, the indicative data stored in the selected memory concerned is read, and it outputs to a latch circuit 213 as an indicative data 212.
[0065] When the bus control signal 206 is "yes", the bus selector 211 changes the output bus 212 and a data bus 210 into a connection condition for the display data bus 107 and a data bus 209 again. On the other hand, when the bus control signal 206 is 'low", the output bus 212 and a data bus 209 are connected for the display data bus 107 and a data bus 210 again.
[0066] A latch circuit 213 stores an indicative data 212 temporarily according to the latch clock 214. The latch circuit 213 has composition outputted to the column circuit 110 by making the this memorized data into the indicative-data signal 126 after this.
[0067] The "selection electrical-potential-difference terminal", the "non-choosing electrical-potential-difference terminal", and the "gradation electrical-potential-difference terminal" which are said in a claim are equivalent to the terminal with which a power circuit 109 outputs a selection electrical potential difference, a non-choosing electrical potential difference, and a gradation electrical potential difference and the signal line connected to this, and a bus in this example. "X electrode switching means" is equivalent to the switch groups 118-121. Moreover, the group who divided X electrode is specified by whether it connects with which switch group.
[0068] The "1st memory" and the "2nd memory" are equivalent to memory 207 and memory 208 in this example. "A write-in means" and a "read-out means" are realized in the bus which connects the clock control section 201, the memory control section 202, the bus selector 211, and these cooperating closely, and operating. The "control means" whose "selection directions means" is a thing equivalent to a clock 201 is realized in the memory control section 202, the clock control section 201, and the bus selector 211 cooperating and operating.
[0069] Actuation of the liquid crystal display of this example is explained.
[0070] First, actuation of the display controller 102 and the column circuit 110 is explained using drawing 2 thru/or drawing 5 . Here, the case where the indicative data stored in memory 208 is read in parallel to this is explained, writing the indicative data 107 inputted from the outside in memory 207.
[0071] The blank signal 105 is set to the low level which means "it is effective." Then, the memory control circuit 203 makes the bus control signal 206 "yes." Moreover, while it can come, simultaneously the memory control section 203 "confirms" the write enable signal in the memory control signal 204, the address which stores the data concerned is specified.
[0072] Then, the bus selector 211 outputs an indicative data 107 to memory 207 because the bus control signal 206 became "yes." In response, memory 207 stores the indicative data concerned in the address specified in the memory control signal 204.
[0073] In this case, if the data which it is going to write in are the first data (0th data), the memory control circuit 203 will specify address"0." The address 80 is specified to the following data (1st data). Furthermore, to the 2nd data inputted into this degree, the address 240 is specified for the address 160 to the 3rd data. The 4th data specify the address 1. To the 5th data, the address 241 is specified [the address 81] for the address 161 to the 7th data to the 6th data. That is, after shifting each group's start address 80 or more, the address is incremented one time every [1] in each groove.
[0074] By addressing in this way, the data outputted to X electrode through the 1st switch group 118 will be stored in the field from the address 0 to the address 79 as shown in drawing 5 R> 5. Moreover,

the data outputted through the 2nd switch group 119 will be stored in the field to the addresses 80–159. Similarly, in the addresses 160–239, the data corresponding to the 4th switch group 121 in the data corresponding to the 3rd switch group 120 are stored in the addresses 240–319 again.

[0075] In parallel to write–in actuation of the indicative data to the memory 207 described above, the output to the latch circuit 213 of the data stored in memory 208 is also performed.

[0076] In drawing 3 , if Horizontal Synchronizing signal 104 becomes "effective", the clock control section 201 will output 80 read–out clocks in the memory control signal 202 (not shown) at a time.

[0077] Moreover, the memory control section 203 specifies the address which reads data in the memory control signal 205 synchronizing with this read–out clock. Sequential increment of the assignment of the address in this case shall be carried out every [1] from the address 0.

[0078] Then, the indicative data corresponding to the 1st switch group 118 is outputted to the beginning through the bus selector 211 to a latch circuit 213 from memory 208. Then, the sequential output of the data corresponding to the 2nd switch group 119, the 3rd switch group 120, and the 4th switch group 121 is carried out.

[0079] A latch circuit 213 memorizes the outputted data synchronizing with the latch clock 214. A latch circuit 213 continues outputting the latched data to the display data bus 126 until the following latch clock 214 becomes effective.

[0080] After outputting 80 read–out clocks, the clock control section 201 "confirms" the output clock contained in the column control signal 115. In addition, this output clock is for directing the timing which outputs a gradation electrical potential difference to the column circuit 110. Moreover, in the clock control section 201, in parallel to this, other switch groups turn ON at OFF the switch group to which the data currently outputted as an indicative data 126 correspond then with the switch control signals 122–125 again. For example, if the indicative data 126 at that time is a thing (it sets to drawing 5 and they are the addresses 80–159) corresponding to the 1st switch group 118, the 1st switch group 118 will be turned ON and the 2nd, 3rd, and 4th switch group 119,120,121 will be turned OFF. By this, the column circuit 110 will output the gradation electrical potential difference corresponding to the indicative–data signal 126 at that time only to a period until the following output clock becomes effective, and predetermined X electrode. In addition, since the column circuit 110 finishes outputting the gradation electrical potential difference corresponding to a front indicative data, the timing of the output of the switch control signals 122–125 will not be especially limited, if it is until it starts the output of the gradation electrical potential difference of the next **********. It does not matter even if it is after starting the output of the gradation electrical potential difference of an indicative data made into the purpose depending on the case. What is necessary is suitably, just to set up in accordance with the property of an actual each part circuit etc.

[0081] While the gradation electrical potential difference is impressed to X electrode (electrodes x0, x4, x8, --, x316) through the 1st switch group 118, the data (it sets to drawing 5 and they are the addresses 80–159) corresponding to the 2nd switch group 119 are read from memory 208. After this, similarly, while the gradation electrical potential difference is outputted through the 2nd switch group 119 Data corresponding to the 3rd switch group 120 (in drawing 5) While the gradation electrical potential difference is further outputted for read–out of the addresses 160–239 through this 3rd switch group 120, read–out of the data (it sets to drawing 5 and them are the addresses 240–319) corresponding to the 4th switch group 121 is performed. The 4th control signal 125 is made into an invalid before the common circuit 112 chooses the following Y electrode. Thus, the writing to the memory 207 of an indicative data 107 and the output of the indicative data 126 from memory 208 finish by one line.

[0082] Then, if following Horizontal Synchronizing signal 104 becomes effective, an indicative data 107 will be shortly written in memory 208. And the indicative data of the following line is read from memory 207. Thus, by repeating read–out / write–in actuation by turns between memory 207,208, from the display controller 102, it is late for an indicative data 107 during 1 level period, and the indicative data

126 is outputted.
[0083] By repeating the above actuation, the gradient electrical potential difference corresponding to an indicative data is outputted to a liquid crystal panel 101 one by one.
[0084] Next, actuation of the common circuit 112 is explained using drawing 1 and drawing 6 .
[0085] If the Rhine signal which directs the change of the first line marker (it abbreviates to "FLM" hereafter) which shows the first Rhine among the common control signals 117, and selection Rhine like drawing 6 becomes effective, the common circuit 112 will output a selection electrical potential difference to an electrode y0 through the output bus 116. On the other hand, a non-choosing electrical potential difference is outputted to other Y electrodes (here electrodes y1-y239). Then, only the switching element of an electrode y0 will be in switch-on. Consequently, the gradation electrical potential difference currently then impressed to X electrode is impressed only to the pixel of the line corresponding to an electrode y0.
[0086] If the Rhine signal becomes effective next time, the common circuit 112 will output a selection electrical potential difference to an electrode y1 shortly. A non-choosing electrical potential difference is outputted to an electrode y0 and electrodes y1-y239. Thereby, the gradation electrical potential difference currently then impressed to X electrode is impressed only to the pixel of the line corresponding to an electrode y1. The display for one screen completes this actuation because even an electrode y239 repeats. Then, the display controller 102 confirms FLM and outputs a sequential selection electrical potential difference from an electrode y0 again.
[0087] As mentioned above, it enables the liquid crystal display of this example to perform the display corresponding to an indicative data by repeating the described actuation.
[0088] The 2nd example of this invention is explained using drawing 10 from drawing 7 .
[0089] The points performed by the input of the indicative data to a display controller and the output of this example of the indicative data from a display controller being parallel differ in an example 1. In addition, the following explanation may be given focusing on difference with an example 1, and explanation may be omitted about the same functional division.
[0090] An outline is explained first.
[0091] the column circuit 704 for driving X electrode of a liquid crystal panel 701 and a liquid crystal panel 701 as the liquid crystal display of this example is shown in drawing 7 , the common circuit 112 for driving Y electrode of a liquid crystal panel 701, the display controller 702 that operates the column circuit 704 and the common circuit 112 according to the indicative data inputted from the outside, and a power circuit 109 -- since -- it is constituted. Moreover, between the column circuit 704 and X electrode of a liquid crystal panel 701, it has the same configuration as the switch groups 118-121 in an example 1, and the switch groups 707-710 are formed in it. Naturally, these and below-mentioned each part are connected by the signal line for delivering and receiving various signals etc., and the bus.
[0092] A liquid crystal panel 701 is the thing of the active-matrix mold of 960 pixel x240 line.
[0093] Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105, the dot clock 106, and the indicative data 703 are inputted into the display controller 702. The display controller 702 is generating and outputting the alternating current-ized signal 108, the column control signal 115, the common control signal 117, an indicative data 705, and the switch control signals 122-125 that control the switch groups 707-710 based on these inputs.
[0094] Synchronizing with a dot clock 106, as for the indicative data 703 in this example, 3 pixels is transmitted to coincidence (parallel). The display controller 702 rearranges this indicative data 703 into the sequence corresponding to each switch groups 707-710, and is outputting it to the column circuit 110 by making this into an indicative data 705. 3 pixels is sent to coincidence also for the indicative data 705 at parallel. Naturally the display data bus 703,705 is a thing corresponding to this.
[0095] The column circuit 704 memorizes an indicative data 705, is outputting the gradation electrical potential difference corresponding to the this memorized indicative data from the output bus 706 synchronizing with the output clock in the column control signal bus 115, and makes the display to a

liquid crystal panel 701 perform. The column circuit 704 of this example can memorize the indicative data 705 to which the amount of 3 pixels collect into, and it is sent at a time. Since the column circuit 704 is equipped with the output of 240 pieces, this column circuit 704 is repeating this storage actuation 80 times, and it has memorized the indicative data for 240 outputs.

[0096] About the common circuit 112 and a power circuit 109, since it is the same as that of an example 1, explanation is omitted.

[0097] Next, the display controller 702 is further explained to a detail using drawing 8 R> 8.

[0098] The display controller 702 is constituted including the output bus 812 of the data bus 809,810 of memory 807 and 808 and memory 807,808 with which the clock control section 201, the memory control section 801, the latch clock bus 802, the data latch circuit 803, a bus 804, the memory control signal bus 805,806, and each can memorize the indicative data for one line, the bus selector 811, and the bus selector 812, the data latch circuit 813, and the bus control signal line 206 as shown in drawing 8 .

[0099] The memory control section 801 is generating the latch clock 802 and the memory control signals 805 and 806 based on the memory system control signal 202 supplied from the clock control section 201. And it passes through the latch clock 802 data latch circuit 803, and it is outputting the memory control signal 805,806 to memory 807,808. The latch clock 802 specifies the timing of incorporation of the indicative data 705 based on the data latch circuit 803, and the signal which synchronized with the dot clock 106 is included. The memory control signals 805 and 806 are constituted including the signal for specifying and changing the operating state (read-out/writing) of memory 807 and 808, respectively, the clock for specifying the timing of read-out/writing, and the address that performs read-out/writing.

[0100] The data latch circuit 803 is for rearranging the indicative data 703 inputted by parallel every 3 pixels corresponding to the switch groups 707-710. This data latch circuit 803 is outputting the indicative data after standing in a line and changing from the output bus 804. The data latch circuit 803 is further explained to a detail using drawing 9 after this. The "conversion means" said in a claim is equivalent to this data latch circuit 803 in this example.

[0101] Memory 807,808 can store the indicative data for one line, respectively. The operating state (writing/readout) is changed by the memory control signal 805,806 into which this memory 807,808 is inputted from the memory control section 801. Moreover, I/O of an indicative data is performed through a data bus 809,810.

[0102] Storing of the indicative data 804 to memory 807,808 is performed synchronizing with the clock in the memory control signal 805,806. Moreover, read-out of the indicative data from memory 807,808 has composition performed synchronizing with the read-out clock of the memory control signal 805,806.

[0103] The bus selector 811 is for changing the connection relation between the output bus 804, the output bus 812, a data bus 809, a data bus 810, and ** according to the bus control signal 206. That is, in reading an indicative data from memory 808 while an indicative data 804 is stored in memory 807, it connects the output bus 812 and a data bus 810 for the output bus 804 and a data bus 809 again. On the contrary, from memory 807, while an indicative data 804 is stored in memory 808, in reading an indicative data, it connects the output bus 8112 and a data bus 809 for the output bus 804 and a data bus 810 again.

[0104] A latch circuit 813 latches the indicative data read from memory 807 (or 808) through the output bus 812, and outputs it as an indicative data 705. The latch is performed according to the latch clock 214. The output of an indicative data 705 is performed synchronizing with the data transfer clock contained in the column circuit control signal 115.

[0105] The data latch circuit 803 is further explained to a detail using drawing 9 .

[0106] The data latch circuit 803 consists of latch circuits 901-904, latch circuits 910-913, output buses 905-908, output buses 914-917, and a data selector 918.

[0107] Latch circuits 901-904 and latch circuits 910-913 can latch the indicative data for 3 pixels at a time. Each output bus 905-908 and the output buses 914-917 to an output of the latched data is

possible for these.
[0108] The data selector circuit 918 chooses a predetermined thing out of the indicative data outputted through the output buses 914-917, and outputs it by making this into an indicative data 804 synchronizing with the latch clock 802. This selection is performed in sequence from which an indicative data 804 becomes a thing corresponding to the switch groups 707-710. The sequence of this selection is specified in fact with the latch clock 802 which the memory control section 801 outputs. The detail of this assignment is performed in explanation of operation.
[0109] Actuation of this example is explained using drawing 7 - drawing 10 . Explanation here is given centering on the display controller 702.
[0110] In drawing 8 , an indicative data 703 is sent to the display controller 702 synchronizing with a dot clock 106. Then, the data latch circuit 803 latches the indicative data for 4 times, i.e., 12 (3x4) pixel, for an indicative data 703 according to the latch clock bus 802. Furthermore, the indicative data for latched 12 pixels is rearranged into the sequence corresponding to the switch groups 707-710, and the data latch circuit 803 outputs it as an indicative data 804.
[0111] Every 3 pixels of indicative datas to which this indicative data 804 belongs to one certain switch group are gathered. That is, the 3-pixel partial output only of the data corresponding to the 1st switch group 707 is carried out to the beginning. Then, the 3-pixel partial output only of the data corresponding to the 2nd switch group 708 is carried out. After this, only every 3 pixels only of data corresponding to the 3rd switch group and the 4th switch group are outputted similarly, respectively. In addition, actuation of the data latch circuit 803 is further explained to a detail after this using drawing 9 and drawing 10 .
[0112] This indicative data 804 is stored in either among memory 807 and memory 808. If the bus control signal 206 is a "low", the bus selector 811 makes switch-on the output bus 804 and the output bus 809. Therefore, the indicative data 804 outputted from the data latch circuit 803 at this time is written in memory 807. When the bus control signal 206 is "yes", the indicative data 804 outputted at this time is written in memory 808.
[0113] Corresponding to each switch groups 707-710, the memory control section 801 specifies the address which writes in data. For example, since the first data for 3 pixels are a thing corresponding to the 1st switch group 707, they specify the address 0. Since the continuing data for 3 pixels are a thing corresponding to the 2nd switch group 708, they specify the address 80. The address 240 is specified as the data corresponding to the 4th switch group 710 for the address 160 at the continuing data corresponding to the 3rd switch group 709. Since the liquid crystal panel of this example is equipped with 960 X electrodes, the initial value of the address assigned to each switch group needs to open or more 80 spacing.
[0114] In addition, in drawing 10 , the memory control section 801 confirms the write enable signal of the memory control signal 805 synchronizing with falling of 5 clock eye of a dot clock 106, after the blank signal 105 becomes effective. And it synchronizes with a dot clock 106 henceforth, and it is the condition (effective (low)/invalid (yes) is controlled.) of a write enable signal. By drawing 10 , the indicative data 804 was written in memory 807, and the situation in case read-out actuation described below to memory 808 is performed was shown.
[0115] In parallel to the above storing actuation, read-out of the indicative data from memory 808 and the transfer to the column circuit 704 are performed.
[0116] The address of the data to read is specified by the memory control signal 806 inputted from the memory control section 801. If Horizontal Synchronizing signal 104 becomes effective, the memory control section 801 will carry out sequential increment of the this specified address from 0 to 79 synchronizing with the read-out clock in the memory system control signal 202. The mask of this read-out clock is carried out after 80 clock output. The read data are outputted to the data latch circuit 813 through the output bus 810, the bus selector 811, and the output bus 812.
[0117] The data latch circuit 813 latches this indicative data 812 according to the latch clock 214. Then, this is outputted to the column circuit 704 as an indicative data 705 synchronizing with the data transfer

clock in the column circuit control signal 115.
[0118] The column circuit 704 carries out the sequential storage of the indicative data 705. And if the output clock of the column control signal bus 115 becomes effective, a gradation electrical potential difference will be outputted to the output bus 706.
[0119] After an output clock becomes effective, a read-out clock becomes "effective" by 80 clocks again. The memory control section 801 makes the indicative data from address "80" to "159" read from memory 808 at this time. After this, the same processing is repeated.
[0120] By repeating the above read-out actuation, the gradation electrical potential difference corresponding to the indicative data for one line stored in memory 808 can be outputted.
[0121] Next, actuation of the data latch circuit 803 is further explained to a detail using drawing 9 and drawing 10 .
[0122] Here, in order to clarify the location displayed on a liquid crystal panel 701, it is made ****** which gives a number called n-m to an indicative data. When n divides 960 X electrodes (an electrode x0 - electrode x959) every four sequentially from left-hand side, the field where the electrode with which the indicative data concerned is outputted belongs is the number which shows the field of what position it is from left-hand side. m is a number which shows in what position the electrode with which the indicative data concerned is outputted is located from left-hand side in the field. However, m shall begin from n and0. The location in the inside of the whole X electrode of the electrode with which a certain indicative-data n-m is outputted can be expressed with 3 n+m. In other words, indicative-data n-m is data outputted to Electrode x (3 n+m). For example, an indicative data 0-0 is an indicative data of the electrode x0 of a liquid crystal panel 701. An indicative data 0-1 should be outputted to an electrode x1, and an indicative data 0-2 should be outputted to electrode x2.
[0123] As for each part of the data latch circuit 803, the timing of operation is determined according to the latch clock 802. Five kinds of latch clocks (each is hereafter called "1st latch clock "-" 5th latch clock") are contained in this latch clock 802.
[0124] The 1st - the 4th latch clock are confirmed for every four cycle of a dot clock 106 as shown in drawing 10 . In an order from the 1st clock, these are behind in the one-cycle [every] phase of a dot clock 106. The 5th latch clock is made effective [once] for every four cycle of dot KURO@KKU 106. This 5th latch clock is behind the 4th latch clock in the phase by the half cycle of a dot clock 106.
[0125] In drawing 10 , if the blank signal 105 becomes effective, synchronizing with falling of the beginning of a dot clock 106, the 1st latch clock will become effective. Then, a latch circuit 901 latches the indicative data 0-0 of the indicative datas 703 - an indicative data 0-2 synchronizing with this. this -- then, a latch circuit 902 - a latch circuit 904 latch the indicative data for 12 pixels to an indicative data 1-0 to 3-2 similarly synchronizing with the 2nd latch clock - 4th latch clock.
[0126] Latch circuits 901-904 output this latched indicative data at a time at latch circuits 910-914 synchronizing with the 5th latch clock. Outputting latch circuits 910-914 is continued from the output buses 914-917 until it latches this and the 5th latch clock becomes "effective" next time.
[0127] A data selector 918 chooses from latch circuits 901-904 only the indicative-data train (1 here the electrodes x0, x4, and x the indicative data 0-0, 1- which corresponded eight times two -2) corresponding to the 1st switch group 707 among the data for 12 pixels outputted to coincidence, and outputs it to the bus selector 811 by making this into an indicative data 804. The output in this case is performed synchronizing with the next 1st latch clock.
[0128] Then, a data selector 918 chooses only the indicative-data train corresponding to the 2nd switch group 708, and outputs it to the bus selector 811 by making this into an indicative data 804. The output in this case is performed synchronizing with the 2nd latch clock. A data selector 918 outputs the indicative data corresponding to the 4th switch group 710 for the indicative data corresponding to the 3rd switch group 709 as an indicative data 804 like the following synchronizing with the 4th latch clock synchronizing with the 3rd latch clock.
[0129] According to the 2nd example explained above, it is parallel, and it can respond to highly minute-

ization of a liquid crystal panel, without changing column circuit 704 grade also to the indicative data inputted.

[0130] The 3rd example of this invention is explained.

[0131] As for this 3rd example, an asynchronous point differs [the data reading clock from memory, and the data write-in clock to memory] from the 2nd example mutually.

[0132] The liquid crystal display of this example is constituted including a liquid crystal panel 701, the column circuit 704 for driving X electrode of a liquid crystal panel 701, the common circuit 112 for driving Y electrode of a liquid crystal panel 701, the display controller 1101 that operates the column circuit 704 and the common circuit 112 according to the indicative data inputted from the outside, a power circuit 109, and the switch groups 707-710 as shown in drawing 11 . Furthermore, the display controller 1101 is equipped with the oscillator 1102 which supplies an external clock 1103 in this example. This external clock 1103 is made into the radical of the read-out clock of the indicative data from memory as it is mentioned later.

[0133] The external clock 1103 into which the display controller 1101 is inputted from an oscillator 1102 in addition to the various input signals 103,104,105,106 and an indicative data 703 is inputted as already stated. Based on these inputs, the display controller 1102 generates an indicative data 705 and the various signals 115,122 - 125,108,117 grades, and is outputting them synchronizing with an external clock 1103.

[0134] The detail of the display controller 1101 is explained using drawing 12 .

[0135] The display controller 1101 is constituted including the clock control section 1201, the clock control section 1203, the memory control section 1205, the bus selector 1208, memory 1213 and 1214, the data latch circuit 803, and the data latch circuit 813 as shown in drawing 12 . Moreover, between these each part was connected and it has the various buses for performing transfer of data and a signal, and a signal line. In addition, in order to simplify drawing, in drawing 12 , the signals 115,122-125,108,117 in drawing 11 are packed, and it is drawing as a signal 1126.

[0136] The clock control section 1201 generates the write-in control signal 1202 and the latch clock 802 based on Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105, and dot KURO@KKU 106.

[0137] Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, and the write-in clock are contained in the write-in control signal 1202. Vertical Synchronizing signal 103 and Horizontal Synchronizing signal 104 are used in order that the memory control section 1205 may judge the data of how many lines an indicative data 804 is. A write-in clock is for an indicative data 804 to tell the memory control section 1205 about the effective time amount range.

[0138] The clock control section 1203 generates the memory reading control signal 1204 which synchronized with the external clock 1103, a signal 1216, and the latch clock 214.

[0139] The memory control section 1205 controls the writing of the data to memory 1213 and 1214, and read-out of the data from these. This memory control section 1205 has composition which generates the memory write-in control signal 1206 which synchronized with the dot clock 106, the memory reading control signal 1207 which synchronized with the external clock 1103, and the bus control signal 206 based on the write-in control signal 1202 and the reading control signal 1204, and outputs this to a selector 1208.

[0140] The memory write-in control signal 1206 and the memory reading control signal 1207 consist of the lead enable signal, a write enable signal, an address signal, and a data signal, respectively (refer to drawing 13). A read-out enable signal is to show read-out completion. In addition, the bus control signal 206 and the lead enable signal are outputted also to the clock control section 1203 through the bus 1204.

[0141] The data latch circuit 803 and the data latch circuit 813 have the same function as an example 2.

[0142] Memory 1213 and 1214 is equipped with the capacity which can memorize the indicative data for ******** 1 screen. The method of arrangement of the indicative data within memory 1213 and 1214 is

the same as that of examples 1 and 2 fundamentally (refer to drawing 5). However, in this example, it is what has arranged the data of each Rhine side by side by the number of the scanning line of a liquid crystal panel (this example 240 duties) as it is shown in drawing 14 , in order to memorize data by one screen. Arrangement of such data is realized by the method of assignment of the address from the memory control section 1205.

[0143] The bus selector 1208 changes the connection relation between a bus 804, a bus 1215, and a bus 1211 and a bus 1212 according to the bus control signal 206. Moreover, the connection relation between the write-in control signal bus 1206, the read-out control signal bus 1207, and the memory control buses 1209 and 1210 is changed.

[0144] When the bus control signal 206 of this bus selector 1208 is "yes", an indicative data 804 is written in memory 1213, and read-out of an indicative data is made to be performed from memory 1214. That is, it writes in with the memory control bus 1209, and let the output bus 8804 and a data bus 1211 be switch-on for the control signal bus 1206 again. Furthermore, let the memory control bus 1210 and the memory-write-signals bus 1207 be switch-on for the output bus 1215 and the memory data bus 1212 again.

[0145] On the other hand, when the bus control signal 206 is a "low", an indicative data 804 is written in memory 1214, and read-out of an indicative data is made to be performed from memory 1213. That is, it writes in with the memory control bus 1210, and let the output bus 804 and a data bus 1212 be switch-on for the control signal bus 1206 again. Furthermore, let the memory control bus 1209 and the memory-write-signals bus 1207 be switch-on for the output bus 1215 and the memory data bus 1211 again.

[0146] Actuation of this example is explained using drawing 13 .

[0147] In drawing 11 , actuation of this example is the same as that of an example 2 except the alternating current-ized signal 108, the column control signal bus 115, the common control signal bus 117, the 1st control signal 122, the 2nd control signal 123, the 3rd control signal 124, the 4th control signal 125, and an indicative data 705 being outputted synchronizing with an external clock 1103. Therefore, only the interior action of the display controller 1101 is explained here.

[0148] The clock control sections 1201 and 1203 are outputting the various signals 802, 1202, 11204, 214, and 1216 based on the signals 103, 104, 105, 106, and 1103 inputted from the outside.

[0149] Moreover, the memory control section 1205 reads with the write-in control signal 1202, from the control signal 1204, generates the memory write-in control signal 1206 and the memory reading control signal 1207, and is outputting them to the selector 1208. Moreover, the bus control signal 206 is outputted to the selector 1208.

[0150] The data latch circuit 803 incorporates an indicative data 703 synchronizing with the latch clock 802 inputted from the clock control section 1201, and after putting in order and changing this, it outputs it as an indicative data 804 corresponding to each switch groups 707-710. The detail of this rearrangement is the same as an example 2. The data for 3 pixels corresponding to one certain switch group are outputted as an indicative data 804 one by one for every switch group.

[0151] The memory control section 1205 makes the indicative data 804 for one screen store in either of memory 1213 and memory 1214 by the selector 1208. Moreover, the indicative data for one screen is made to read from memory 1213 (or 1214), being outputted from the clock control section 1203, reading in parallel to this, and synchronizing with a clock. Read-out of this indicative data is performed like other examples from the memory of the direction where write-in actuation of data is not then performed.

[0152] The data latch circuit 813 latches the indicative data read from memory 1213 (or 1214) synchronizing with the latch clock 214. And synchronizing with the transfer clock contained in the column control signal 115 (drawing 12 signal 1216), an indicative data is outputted as an indicative data 705.

[0153] If read-out is completed, the memory control section 1205 will make the lead enable signal in the memory control signal 1207 an invalid (this example "low"), as shown in drawing 13 . The clock control

section 1203 which received this lead enable signal stops the output of a read-out clock.
[0154] The memory control section 1205 changes the condition (yes, /low) of the bus control signal 206 as it is shown in drawing 13 , when read-out from storing in memory 1213 and memory 1214 of the indicative data for one screen is completed.
[0155] Then, a selector 1208 will operate corresponding to this and the memory in which an indicative data 804 is stored, and the memory from which an indicative data is read will interchange next time. Moreover, the clock control section 1203 initializes oneself corresponding to the status change of the bus control signal 206. And it prepares for the display of degree screen and generation of a signal 1216 is begun again. Furthermore, the clock control section 1203 resumes the output to the memory control section 1205 of a read-out clock. The memory control section 1205 which received this read-out clock reads an indicative data from address "0" one by one synchronizing with this read-out clock.
[0156] being possible in the display to a liquid crystal panel 701, though the liquid crystal display of this example has two asynchronous clocks by repeating the above actuation -- ** -- it is carrying out.
[0157] The 4th example is explained.
[0158] This 4th example arranges the switch group which chooses the output of a common circuit between a common circuit and Y electrode of a liquid crystal panel, and the points which control this by the display controller differ in the example 1. About other points, it is the same as that of an example 1 fundamentally. It is applied when this example has few outputs of a common circuit than the number of Rhine of a liquid crystal panel.
[0159] The liquid crystal display of this example is explained using drawing 15 .
[0160] Liquid crystal panel 101 the very thing is the same as that of an example 1. However, Y electrode which it has 240 is divided into two groups, and impression of its selection / non-choosing electrical potential difference is controlled by this example. Hereafter, Y electrode located in the field of a lower half on the other hand with the 1st common bus 1610 in Y electrode located in the field of the upper half in drawing 15 is called the 2nd common bus 1611.
[0161] The switch groups 1606-1609 are for changing the connection relation between Y electrode of a liquid crystal panel, the output bus 1604 of the common circuit 1603, and the non-choosing electrical-potential-difference signal line 1605 from a power circuit 109.
[0162] The non-choosing electrical potential difference which a power circuit 109 generates is outputted even if it leads the non-choosing electrical-potential-difference signal line 1605 which branched and has come out of the middle of the scan electrical-potential-difference bus 113. This non-choosing electrical-potential-difference signal line 1605 is constituted possible [the 2nd common bus 1611 and connection] through the 4th switch group 1609 with the 1st common bus 1610 of a liquid crystal panel again through the above-mentioned 2nd switch group 1607.
[0163] Otherwise, the common circuit 1603 outputs a non-choosing electrical potential difference for a selection electrical potential difference to either among the output terminals y0-y119 which constitute the output bus 1604. It is directed by the common control signal 1602 inputted from the display controller 1601 whether to output a selection electrical potential difference from which output terminal.
[0164] The output bus 1604 of the common circuit 1603 of this example is connectable with the 2nd common bus 1611 through the 1st common bus 1610 and the 3rd switch group 1608 through the 1st switch group 1606.
[0165] The display controller 1601 is generating and outputting the common control signal 1602 for controlling the common circuit 1603. Furthermore, it has composition which outputs the 1st control signal 1612 for controlling the switch groups 1606-1609, and the 2nd control signal 1613. The clock control section 201 of drawing 2 is generating these control signals 1612 and 1613. The internal configuration of the display controller 1601 is the same as that of drawing 2 fundamentally. Naturally, the 1st control signal 122 for controlling the switch groups 118-121 - the 4th control signal 125 are also outputted.
[0166] The 1st switch group 1606 and the 4th switch group 1609 are turned ON, and, on the other hand,

the display controller 1601 turns OFF the 2nd switch group 1607 and the 3rd switch group 1608, when impressing a selection electrical potential difference to either of the Y electrodes belonging to the 1st common bus 1610. Thereby, the output from the common circuit 1603 is impressed to the 1st common bus 1610, and the non-choosing voltage signal 1605 is impressed to the 2nd common bus 1611. On the contrary, in impressing a selection electrical potential difference to either of the Y electrodes belonging to the 2nd common bus 1611, the 1st switch group 1606 and the 4th switch group 1609 are turned OFF, and, on the other hand, it turns ON the 2nd switch group 1607 and the 3rd switch group 1608. Thereby, the non-choosing voltage signal 1605 is impressed to the 1st common bus 1610, and the output from the common circuit 1603 is impressed to the 2nd common bus 1611.

[0167] "Y electrode switching means" said in a claim is realized by the switch groups 1606-1609. The "group" of Y electrode is equivalent to the 1st common bus 1610 and the 2nd common bus 1611.

[0168] Actuation of this example is explained using drawing 15 and drawing 16 .

[0169] Actuation of this example is fundamentally the same as the 1st example of the above except actuation of the common circuit 1603. Therefore, only actuation of the common circuit 1603 is explained here.

[0170] "during the period which should choose either of the Y electrodes belonging to the 1st common bus 1610, and the display controller 1601 -- the 1st control signal 1612 -- it is effective" [(yes)] -- moreover, let the 2nd control signal 1613 be an "invalid" (low). Consequently, the 1st switch group 1606 and the 4th switch group 1609 are turned on (switch-on), and, on the other hand, the 2nd switch group 1607 and the 3rd switch group 1608 are turned off (cut off state). In this condition, the non-choosing electrical potential difference 1605 will be impressed to Y electrode with which the selection / non-choosing electrical potential difference 1604 which the common circuit 1603 outputs to Y electrode belonging to the 1st common bus 1610 belong to the 2nd common bus 1611 on the other hand. The common circuit 1603 synchronizes with the Rhine signal the output terminal which outputs a selection electrical potential difference in the meantime, and is y0->y1->y2-> one by one... It is changing with ->y199 and is scanning within the limits of the 1st common bus 1610.

[0171] the "display controller 1601 after the scan to Y electrode (electrodes y0-y119) belonging to the 1st common bus 1610 finishes (that is, after choosing an electrode y199) -- next time -- the 2nd control signal 1613 -- it is effective" [(yes)] -- moreover, let the 1st control signal 1612 be an "invalid" (low). Consequently, the 1st switch group 1606 and the 4th switch group 1609 are turned off (cut off state), and, on the other hand, the 2nd switch group 1607 and the 3rd switch group 1608 are turned on (switch-on). In this condition, the selection / non-choosing electrical potential difference 1604 which the common circuit 1603 outputs will be impressed to Y electrode with which the non-choosing electrical potential difference 1605 belongs to the 2nd common bus 1611 on the other hand at Y electrode belonging to the 1st common bus 1610. Consequently, Y electrode with which the selection electrical potential difference which the common circuit 1603 outputs is impressed is y120->y121->y122->... It will be changed one by one with ->y239.

[0172] In addition, based on the timing of FLM and the Rhine signal, effective (yes) is performed and the display controller 1601 is making an invalid (low) change of the 1st control signal 1612 and the 2nd control signal 1613. In the example shown in drawing 16 , the common circuit 1603 outputs a selection electrical potential difference to an output terminal y0 ignited by the Rhine signal becoming effective during the period when the FLM signal in the common control signal 1602 has become yes. It is a time of impressing a selection electrical potential difference to an electrode y120 that the common circuit 1603 outputs a selection electrical potential difference to an output terminal y0 next time, after the 120 clock partial output of the clock in the Rhine signal 1602 is carried out that is,.

[0173] In this example, even when there are few output buses of the common circuit 1603 than the number of Y electrodes of a liquid crystal panel, an electrode y0 to the electrode y239 of a liquid crystal panel can scan sequentially.

[0174] According to the 1st explained above - the 4th example, it can respond easily to highly minute-

ization of a liquid crystal panel. Moreover, even when there is modification to which the number of pixels and the number of Rhine of a liquid crystal panel are made to increase, according to the increment, it can respond by making the storage capacity of memory increase.

[0175] When there are more effective datas of an indicative data than the number of displays of a liquid crystal panel, it is possible also for displaying on a liquid crystal panel only the field part as which it was beforehand determined of the display images. In order to realize this, the register which memorizes the coordinate value which shows the range of the image field displayed on a liquid crystal panel is prepared in a display controller. And what is necessary is to compare the display position of the inputted indicative data with the coordinate value stored in this register, and to memorize in memory only the indicative data about the image field specified in the register. If it does in this way, an aspect ratio can also display a different image from the liquid crystal panel.

[0176] In the above-mentioned example, although rearranged at the time of the writing to the memory of an indicative data, it reads conversely and may be made to sometimes rearrange. For example, an indicative data is put in order and stored in the order which usually passed and was inputted at the time of writing. And what is necessary is just to increment the address every [4] at the time of read-out, in case a series of indicative datas corresponding to one certain switch group are read. In case the data corresponding to the 1st switch group are read, the addresses 0 and 4 and 8 -- are specified.

[0177] At this example, the display controller has been miniaturized by making it one LSI.

[0178]

[Effect of the Invention] It can respond to highly minute-ization of a liquid crystal panel, without making small the output pitch of a common circuit and column circuit which is a liquid crystal drive circuit according to this invention.

[0179] Also when a write-in clock and a read-out clock are asynchronous clocks, it can respond by having the memory for one screen.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a suitable liquid crystal display controller to display indicative datas, such as a personal computer and a workstation, on a liquid crystal panel.

[0002]

[Description of the Prior Art] By the personal computer and workstation, the liquid crystal display is used widely.

[0003] Hereafter, the configuration and actuation of a liquid crystal display are explained using drawings 1717 , 18, and 19. Horizontal resolution gives explanation here taking the case of the case where the liquid crystal panel 640 pixels per each pixel of R, G, and B (a total of 1920 (= 640x3) pixels) and whose vertical definition are 480 lines is driven by the display controller (trade name" column circuit

HD66310") by Hitachi, Ltd. in addition -- the contents of this explanation -- the Hitachi LCD driver LSI data book p of the Hitachi, Ltd. semi-conductor operation division issue -- it is indicated by 661 and 662.

[0004] The indicative data 2401 and the synchronizing signal 2402 which synchronized with this are inputted into the driver control means 2110 from the personal computer, the workstation, etc. as shown in drawing 17 . In addition, a dot clock, a Horizontal Synchronizing signal, and a Vertical Synchronizing signal are included in a synchronizing signal 2402.

[0005] The data-conversion circuit 2120 within the driver control means 2110 has changed the indicative data 2401 so that it may double with the interface of the column circuit 2100 mentioned later. And the data after this conversion are outputted as an indicative data 2103 for drivers (refer to drawing 18).

[0006] A frequency divider 2121 is carrying out dividing of the dot clock contained in the synchronizing signal 2402, and an indicative data generates the indicative-data incorporation clock 2111 during an effective period, and it is outputting this (refer to drawing 18).

[0007] Moreover, a delay circuit 2122 delays the Horizontal Synchronizing signal included in the synchronizing signal 2402, and is generating and outputting the indicative-data latch clock 2104 and the enable signal 2105 (refer to drawing 18).

[0008] The indicative data 2103 for drivers and the indicative-data incorporation clock 2111 are outputted to the column circuit 2100 among these signals. On the other hand, the enable signal 2105 is outputted to the scan drive circuit 2131. Indicative-data latch KURO@KKU 2104 is outputted to both the column circuit 2100 and the scan drive circuit 2131.

[0009] The column circuit 2100 incorporates the indicative data 2103 for drivers in falling of the indicative-data incorporation clock 2111. Here, since the column circuit HD 66310 by Hitachi, Ltd. currently used as a column circuit 2100 is what has a-160 output, it is carrying out 12-piece (= 1920/160) use of HD66310 in this liquid crystal display. Hereafter, the column circuit 2100-1 to 2100-12 is generically called the column circuit group 2130. The column circuit 2100 incorporates the indicative data 2103 for drivers, only when the enable signal input EIO1 is a low level.

[0010] Moreover, if this column circuit 2100 incorporates the indicative data for 60 pixels, the enable signal output EIO2 will change from high level to a low level. And the enabling output signal EIO2 of the column circuit 2100 located in left-hand at the enable signal input EIO1 of each column circuit 2100 is inputted. In addition, the enable signal input EIO1 is grounded about the column circuit 2100-1 located in a high-order end. In addition, the back explains the internal configuration of the column circuit HD 66310 more concretely.

[0011] If the column circuit 2100-1 completes incorporation for the indicative data 2103 for 160 pixels, the enabling output signal EIO2 will change from high level to a low level. Then, the column circuit 2100-2 of the next step (right-hand) is enabling. And the column circuit 2100-2 concerned starts incorporation of an indicative data 2103 shortly.

[0012] It incorporates 160 pixels of indicative datas at a time one by one from the column circuit 2100 located in left-hand side similarly hereafter.

[0013] And if it finishes incorporating the indicative data 2103 for drivers for one line, the column Cairo group 2130 will impress the display electrical potential difference corresponding to the indicative data concerned for one line to a liquid crystal panel 2132.

[0014] On the other hand, the scan drive circuit 2131 is scanning vertical lines sequentially synchronizing with an enable signal 2105.

[0015] The indicative data (data which the latch circuit 2303 mentioned later latches) which the column circuit 2100 outputs will be then displayed in Rhine chosen by the scan drive circuit 2131.

[0016] In addition, the writing of data is performed even when an indicative data does not change for every Rhine.

[0017] Next, the outline of the column circuit HD 66310 is explained using drawing 19 .

[0018] It has the composition that this input indicative data 2103 for 4 pixels is parallel, and is inputted in the column circuit HD 66310. The input indicative data 2103 is a gradient data triplet about each pixel. Moreover, it has 160 signal lines 2101 for outputting liquid crystal driver voltage.
[0019] The latch address counter 2301 counts falling of the indicative-data incorporation clock 2111, and generates a latch signal. In addition, the indicative-data incorporation clock 2111 has come to be able to carry out a mask in the enable signal input EIO1. A latch signal is not generated when the enable signal input EIO1 is high-level. Moreover, after counting the indicative-data incorporation clock 2111 40 times, the enable signal output EIO2 is made into a low level. In addition, since the indicative data for 4 pixels can be incorporated at once as mentioned later, 40 counts are equivalent to incorporation of the indicative data for 160 (= 4x40) pixels.
[0020] The latch circuit 2302 is divided into every 4-pixel 40 steps. This latch circuit 2302 incorporates the indicative data 21003 for drivers by 4 pixels to coincidence synchronizing with the latch signal from the latch address counter 2301.
[0021] The latch circuit 2303 consists of latch circuits for 160 pixels. A latch circuit 2303 latches the indicative data which the latch circuit 2302 incorporated synchronizing with the indicative-data latch clock 2104. And one-line time amount maintenance of this latched data is carried out.
[0022] The level-shifter circuit 2304 decodes the indicative data which the latch circuit 2303 latched, and generates the select signal for choosing liquid crystal applied voltage.
[0023] The liquid crystal drive circuit 2305 chooses one of the liquid crystal driver voltages 2306 whose eight kinds exist according to a select signal, and outputs it to X electrode of a liquid crystal panel by making the this chosen electrical potential difference into applied voltage 2101.
[0024] As stated above, the display action in a liquid crystal display is the repeat of the most latch actuation of the indicative data to the column circuit 2100.
[0025] In addition to this, the horizontal direction of a liquid crystal panel is divided into two fields, and there is a thing of transmitting the indicative data for every field to coincidence in the drive method of a liquid crystal display. in this drive method, while it has two display memory and the indicative data is written in one side, an indicative data is read from the display memory of another side, and it is this reading **** -- the indicative data is outputted to parallel. Such a technique is indicated by JP,1-113793,A, JP,2-126285,A, and JP,5-232898,A, for example.
[0026]
[Problem(s) to be Solved by the Invention] A liquid crystal panel is also asked for a highly minute display in current. In order to correspond to this, not only detailed-izing of a pixel pitch but the output pitch of a column circuit must be made detailed. This is because cascade connection which the column circuit mentioned above cannot be performed. Moreover, formation of small area of the column circuit itself, small pitch-ization of TAB which makes liquid crystal panel connection of the output of a column circuit, etc. must be attained.
[0027] However, when TAB and a liquid crystal panel were made detailed, the alignment and the junction technique for the joint will take an advanced technique, and another problem that a production cost became high was produced. Therefore, the technique corresponding to the liquid crystal panel of a highly minute display was searched for, using the conventional liquid crystal drive circuit.
[0028] It aims at offering the display controller which can respond to the liquid crystal panel which made the pixel pitch detailed, the conventional liquid crystal drive circuit being used for this invention.
[0029]
[Means for Solving the Problem] This invention is what was made in order to attain the above-mentioned purpose. As the 1st mode The liquid crystal panel of the active-matrix mold equipped with M Y electrodes and X electrode of N individual, The selection electrical-potential-difference terminal which is equipped with the function which generates a selection electrical potential difference, a non-choosing electrical potential difference, and two or more kinds of gradation electrical potential differences, and outputs the above-mentioned selection electrical potential difference, The power circuit equipped with

the non-choosing electrical-potential-difference terminal which outputs the above-mentioned non-choosing electrical potential difference, and the gradation electrical-potential-difference terminal which outputs the above-mentioned gradation electrical potential difference, The column circuit which is equipped with n output terminals (n<N), chooses for this every output terminal corresponding to the data stream which was able to give separately either of the above-mentioned gradation electrical potential differences outputted from the above-mentioned power circuit, and outputs the this chosen gradation electrical potential difference from the output terminal concerned, The above-mentioned selection electrical potential difference to any one of the above-mentioned Y electrodes Moreover, a common means to impress the above-mentioned non-choosing electrical potential difference to other Y electrodes, A component classifies the above-mentioned X electrode into two or more groups who are n or less pieces, and chooses any one of these groups. X electrode switching means connected with the correspondence relation to which only X electrode belonging to the this selected group was beforehand determined as the above-mentioned output terminal of the above-mentioned column circuit, The indicative data and the Horizontal Synchronizing signal are inputted from the outside at least. The liquid crystal display characterized by having the display controller outputted to the above-mentioned column circuit one by one for every assembly of the indicative data which corresponds mutually is offered.

[0030] The 1st memory the above-mentioned display controller can remember the data for at least one line to be, The 2nd memory which can memorize the data for at least one line, and the write-in means which takes in the indicative data inputted from the outside and is written in the 1st memory of the above, or the 2nd memory, From the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means among the 1st memory of the above, and the 2nd memory at the time A read-out means to begin to read the indicative data already stored in the memory concerned, and to output it one by one for every assembly of the indicative data which corresponds mutually, After the above-mentioned column circuit finishes outputting a gradation electrical potential difference to X electrode belonging to a certain group, selection of the above-mentioned group according to the above-mentioned X electrode switching means before starting the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- with the selection directions means made to change so that the next group's X electrode and the output terminal of a column circuit may be connected It may be constituted including the control means to which the memory made into the object of write-in actuation of the above-mentioned indicative data based on the above-mentioned write-in means is made to be changed by turns between the 1st memory of the above, and the 2nd memory of the above ignited by the above-mentioned Horizontal Synchronizing signal becoming effective.

[0031] It is what is performed by the input from the outside of the above-mentioned indicative data being parallel. Receive only several pixel minutes which was able to define beforehand the indicative data inputted from the above-mentioned outside, and this beam indicative data with a receptacle is classified based on the group to whom X electrode with which the indicative data concerned corresponds belongs. It may have further a conversion means to output for this every classification, and the above-mentioned write-in means may write the indicative data which the above-mentioned conversion means outputs in the 1st memory of the above, or the 2nd memory of the above.

[0032] The above-mentioned write-in means is what performs the above-mentioned write-in actuation synchronizing with the write-in clock generated separately. The above-mentioned read-out means The above-mentioned write-in clock is what performs the above-mentioned read-out synchronizing with the asynchronous read-out clock by which special generation is carried out. The above-mentioned control means The change of memory made into the write-in object of the above-mentioned indicative data based on the above-mentioned write-in means It may check having written in the indicative data for one screen, it may be made to perform instead of the above-mentioned Horizontal Synchronizing signal, and the 1st memory of the above and the 2nd memory of the above may be equipped with the storage capacity which can memorize the indicative data for the liquid crystal panel 1 above-mentioned screen.

[0033] The common circuit which the above-mentioned common means is equipped with m output terminals (m<M), makes sequential selection of one of these output terminals, and outputs a non-choosing electrical potential difference for the selection electrical potential difference above-mentioned [from the this chosen output terminal] from other output terminals, While connecting with the correspondence relation to which only Y electrode which divides the above-mentioned Y electrode into two or more groups whose components are m or less pieces, and belongs to one of groups was alternatively determined as the above-mentioned output terminal of the above-mentioned common circuit beforehand It has Y electrode switching means which connects to the non-choosing electrical-potential-difference terminal of the above-mentioned power circuit Y electrode which is not connected with the above-mentioned common circuit at the time. The above-mentioned display controller it is the thing which makes selection of the above-mentioned group by the above-mentioned Y electrode switching means change every whenever the above-mentioned common circuit finishes choosing all output terminals -- it is desirable.
[0034] As for the 1st memory of the above, and the 2nd memory of the above, being constituted possible [modification of the storage capacity] is more desirable.
[0035] The liquid crystal panel of the active-matrix mold equipped with M Y electrodes and X electrode of N individual as the 2nd mode of this invention, The column circuit which outputs the gradation electrical potential difference corresponding to the data stream which was equipped with n output terminals (n<N) and was separately given from this output terminal, A component classifies the above-mentioned X electrode into two or more groups who are n or less pieces, and chooses any one of these groups. X electrode switching means connected with the correspondence relation to which only X electrode belonging to the this selected group was beforehand determined as the above-mentioned output terminal of the above-mentioned column circuit, In the display controller used for the drive of the liquid crystal display which consisted of ****** The 1st memory which can memorize the data for at least one line, and the 2nd memory which can memorize the data for at least one line, The write-in means which takes in the indicative data inputted from the outside and is written in the 1st memory of the above, or the 2nd memory, From the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means among the 1st memory of the above, and the 2nd memory at the time A read-out means to begin to read the indicative data already stored in the memory concerned, and to output it one by one for every assembly of the indicative data which corresponds mutually, After the above-mentioned column circuit finishes outputting a gradation electrical potential difference to X electrode belonging to a certain group, selection of the above-mentioned group according to the above-mentioned X electrode switching means before starting the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- with the selection directions means made to change so that the next group's X electrode and the output terminal of a column circuit may be connected It carries out an opportunity [the above-mentioned Horizontal Synchronizing signal becoming effective about the memory made into the object of write-in actuation of the above-mentioned indicative data based on the above-mentioned write-in means]. The display controller characterized by being constituted including the control means made to be changed by turns between the 1st memory of the above and the 2nd memory of the above is offered.
[0036]
[Function] The power circuit is outputting [the selection electrical potential difference from a selection electrical-potential-difference terminal] the gradation electrical-potential-difference terminal from a gradation electrical-potential-difference terminal for the non-choosing electrical potential difference from the non-choosing electrical-potential-difference terminal.
[0037] X electrode switching means classified the above-mentioned X electrode into two or more groups who are n or less pieces, and the component has connected it with the correspondence relation to which only X electrode which chooses any one of these groups and belongs to the this chosen group was beforehand determined as the above-mentioned output terminal of the above-mentioned column

circuit.
[0038] A display controller is outputted to the above-mentioned column circuit one by one for every assembly of the indicative data which corresponds mutually. A display controller can be constituted as follows, for example.
[0039] A write-in means takes in the indicative data inputted from the outside, and is writing it in the 1st memory of the above, or the 2nd memory. Among the 1st memory and the 2nd memory, at the time, a read-out means is beginning to read the indicative data already stored in the memory concerned one by one for every assembly of the indicative data which corresponds mutually, and is outputting it from the direction which has not been set as the activation object of the write-in actuation by the above-mentioned write-in means. The control means is making the memory made into the object of write-in actuation of the indicative data based on a write-in means changed by turns between the 1st memory of the above, and the 2nd memory of the above ignited by a Horizontal Synchronizing signal becoming effective at this time. Thereby, by turns, writing/read-out of every one line are performed in the 1st memory and 2nd memory, and an indicative data goes to them. It writes in or rearrangement is performed by specifying this address corresponding to each group, and going in the case of read-out.
[0040] A column circuit outputs the gradation electrical potential difference which chose and this chose either of the gradation electrical potential differences for every output terminal corresponding to the data stream to which it is given from a display controller from the output terminal concerned. selection of the group according to X electrode switching means after finishing outputting a gradation electrical potential difference to X electrode with which a column circuit belongs to a certain group at this time, before the selection directions means of a display controller starts the output of the gradation electrical potential difference corresponding to the next group's X electrode -- this -- it is made to change so that the next group's X electrode and the output terminal of a column circuit may be connected Consequently, the gradation electrical potential difference which is outputting the column circuit then will be impressed to X electrode belonging to the group chosen at this time.
[0041] In addition, when parallel, an indicative data is classified for every group according to a conversion means, and it is made for the input from the outside of an indicative data to make it output for this every classification with it. And a write-in means should just write the indicative data which a conversion means outputs in the 1st memory of the above, or the 2nd memory of the above. moreover, the clock with which a write-in means synchronizes and the clock with which a read-out means synchronizes -- mutual -- asynchronous ** -- in a certain case, a control means checks having written in the indicative data for one screen for the change of memory made into the write-in object of the above-mentioned indicative data based on the above-mentioned write-in means, and is made to carry it out to it. And the 1st memory and 2nd memory of the above are equipped with the storage capacity which can memorize the indicative data for the liquid crystal panel 1 above-mentioned screen.
[0042] On the other hand, a common means impresses the above-mentioned non-choosing electrical potential difference to other Y electrodes for a selection electrical potential difference again any one of the Y electrodes. This common means can be constituted as follows, for example. A common circuit makes sequential selection of one of these output terminals, and is outputting the non-choosing electrical potential difference for the selection electrical potential difference above-mentioned [from the this chosen output terminal] from other output terminals. Y electrode switching means divides Y electrode into two or more groups whose components are m or less pieces, and connects it with the correspondence relation to which only Y electrode belonging to one of groups was alternatively determined as the above-mentioned output terminal of the above-mentioned common circuit beforehand. Moreover, Y electrode which is not connected with the above-mentioned common circuit at the time is connected to the non-choosing electrical-potential-difference terminal of the above-mentioned power circuit. And a display controller makes the selection situation by the above-mentioned Y electrode switching means change every, whenever a common circuit finishes choosing all output terminals.

[0043]
[Example] The example of this invention is explained using a drawing.
[0044] The 1st example of this invention is explained using drawing 6 from drawing 1 .
[0045] the column circuit 110 for driving X electrode of a liquid crystal panel 101 and a liquid crystal panel 101 as the liquid crystal display of this example is shown in drawing 1 , the common circuit 112 for driving Y electrode of a liquid crystal panel 101, the display controller 102 that operates the column circuit 1110 and the common circuit 112 according to various signals, an indicative data, etc. which are inputted from the outside, and a power circuit 109 -- since -- it is constituted. Naturally, these are connected by the signal lines 103, 104, 105, 106,108,127,122-125 for delivering and receiving various signals etc., and buses 111, 113, and 115,126,117,107. Furthermore, in this example, connection between a liquid crystal panel 101 and the column circuit 110 is made through the switch groups 118-121 which operate according to the directions from the display controller 102. This example is characterized [greatest] by to have formed these switch groups 118-121 and the display control corresponding to this.
[0046] In addition, since correspondence relation between an explanatory note and a drawing is made intelligible in the following explanation, the number of the signal line concerned and a bus may be attached and the signal delivered and received through these signal lines or a bus may be called. For example, suppose that the indicative data inputted through a bus 107 is called an indicative data 107. The same is said of explanation of other examples.
[0047] A liquid crystal panel 101 is the thing of the active-matrix mold which constitutes a matrix from 320 X electrodes and 240 Y electrodes, and has a switching element at the intersection.
[0048] The display controller 102 generates the indicative data 126 and the various signals for displaying on a liquid crystal panel 101 based on the indicative data 107 and the various control signals which are inputted from the outside. There are Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105 that shows the scope of an indicative data, and a dot clock 106 in the control signal inputted from the outside. An indicative data 107 synchronizes with a dot clock 106, it is the sequence according to the display position on a screen, and is serial and is sent.
[0049] The display controller 102 is generating and outputting the alternating current-ized signal 108, the column control signal 115, the common control signal 117, an indicative data 126, and the switch control signals 122-125 that control the switch groups 118-121 based on these control signals 103-106 and an indicative data 107.
[0050] The display controller 102 of this example rearranged this indicative data 107 corresponding to the connection relation between the switch group 118 - 121 grades, and is equipped with the function outputted as an indicative data 126. In this example, after rearranging an indicative data corresponding to there being four switch groups, it is dividing and outputting to four groups. This group division is performed by classifying the display position on a screen according to the system of residues of 4. This responds to the connection relation between each switch groups 118-121 and X electrode following the system of residues of 4. Within each group, a display position is more previously outputted by the thing in left-hand side. The detail of this display controller 102 and this rearrangement is explained a back forge fire.
[0051] A power circuit 109 is for generating the various electrical potential differences (the counterelectrode electrical potential difference 127, the gradation electrical potential difference 111, selection / non-choosing electrical potential difference 113) impressed to a liquid crystal panel. The gradation electrical potential difference 111 is generated synchronizing with the alternating current-ized signal 108, and is supplied to the column circuit 110. There are a thing of straight polarity and a thing of negative polarity in this gradation electrical potential difference 111 to the counterelectrode electrical potential difference 127. Selection / non-choosing electrical potential difference 113 is outputted to the common circuit 112.
[0052] The column circuit 110 chooses either for every pixel among the gradation electrical potential

differences inputted through the bus 111, and outputs what was this chosen from the output bus 114 (output terminals s0-s80). This gradation electrical potential difference is then supplied only to predetermined X electrode made into the output bus 114 and switch-on by switch 118 above-mentioned groups 118-121. This column circuit 110 is having the operating state controlled by the column circuit control signal 115 which the display controller 102 outputs.

[0053] The common circuit 112 outputs the selection electrical potential difference / non-choosing electrical potential difference inputted through a bus 113 to Y electrode of a liquid crystal panel 101 through the output bus 116. This common circuit 112 is having the operating state controlled by the common circuit control signal 117 which the display controller 102 outputs.

[0054] The switch groups 118-121 are for changing suitably the connection relation between the output terminals s0-s80 which constitute the output bus 114 of the column circuit 110, and X electrode (electrodes x0-x319) of a liquid crystal panel 101. Each switch groups 118-121 consist of 80 switches, respectively. The electrodes x0-x319 of a liquid crystal panel 101 are divided into four groups by classifying the location from left-hand side according to the regulation (this example 4 system of residueses) which was able to be defined beforehand. The switch groups 118-121 connect only X electrode belonging to one of groups with the output bus 114 of a column circuit suitably by changing an ON/OFF condition according to the directions from control signals 122-125, respectively. Here, the switch belonging to the 1st switch group 118 is called a switch 1-1, a switch 1-2, --, a switch 1-80 sequentially from left-hand side. The switch belonging to the 2nd switch group is called a switch 2-1, a switch 2-2, --, a switch 2-80. The concrete ****** relation of the output terminals s0-s80 which adopt the way of calling with the same said of the switch belonging to the 3rd switch group 120 and the 4th switch group 121, the switch groups 181-121, and electrodes x0-x319 and ** is as follows. The output terminal s0 is connectable with an electrode x3 by the switch 4-1 with electrode x2 with an electrode x1 and a switch 3-1 by the electrode x0 and the switch 2-1 by the switch 1-1. Similarly, electrodes x4, x5, x6, and x7 and connection are possible for an output terminal s1 by the switch 1-2, 2-2, 3-2, and 4-2. Between output terminals s2-s80 and electrodes x8-x319 is connected with the same relation.

[0055] Therefore, the gradation electrical potential difference outputted from output terminals s0-s80 can be impressed to electrodes x0, x4, x8, x12, --, x316 by turning ON only the 1st switch group 118 (switch 1-1 to 1-80), and turning OFF other switch groups 119,120,121. If only the 2nd switch group 119 (switch 2-1 to 2-80) is turned ON, the gradation electrical potential difference similarly outputted from output terminals s0-s80 can be impressed to electrodes x1, x5, x9, x113, --, x317. The same is said of the 3rd switch group 120 (switch 3-1 to 3-80), and the 4th switch group 121 (switch 4-4 to 3-80).

[0056] The condition (ON/OFF) of the 1st switch group 118 is changed by the 1st control signal 122 which the display controller 102 outputs. The condition (ON/OFF) of the 2nd switch group 119 is changed by the 2nd control signal 123. The condition (ON/OFF) of the 3rd switch group 120 is changed by the 3rd control signal 124. The condition (ON/OFF) of the 4th switch group 121 has composition changed by the 4th control signal 125.

[0057] Next, the display controller 102 is further explained to a detail using drawing 2 . The display controller 102 is constituted including the clock control section 201, the memory system control bus 202, the memory control section 203, the memory control bus 204, the memory control bus 205, the bus control line 206, memory 207, memory 208, the data bus 209,210, the bus selector 211, and the latch circuit 213.

[0058] The clock control section 201 generates the alternating current-ized signal 108, the column control signal 115, the common control signal 117, and the switch control signals 122-125 based on Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105, and a dot clock 106. Furthermore, the clock control section 201 is also generating the memory system control signal 202 and the latch clock 214 which control the inside of the display controller 102.

[0059] The memory system control signal 202 is constituted including the read-out clock. The latch clock 214 synchronizes with the data transfer clock in the column control bus 115. Moreover, the data

transfer clock in below-mentioned drawing 4 and drawing 6 and the output clock are contained in the column control signal 115. Moreover, FLM in drawing 6 and the Rhine signal are included in the common control signal 117.

[0060] The memory control sections 203 are the writing of the data to memory 207,208 / thing for reading and controlling the condition of the bus selector 211. Therefore, the memory control section 203 generates the memory control signal 204,205 which synchronized with the memory system control signal 202, and is outputting it to each memory 207,208. The write enable signal in drawing 3 which makes memory 207,208 the condition which can be written in, and the lead enable signal made into the condition which can be read and the address signal which writes in data and specifies the address are contained in the memory control signal 204,205.

[0061] Furthermore, the memory control section 203 is outputting the bus control signal 206 to the bus selector 211. The memory control section 203 makes the bus control signal 206 a "low", when performing the writing to memory 207, performing the bus control signal 206 to "yes" and writing in memory 208 on the other hand.

[0062] Memory 207 and memory 208 have the storage capacity which can memorize the indicative data for one line, respectively. The writing of the data to this memory 207 and 208 and read-out are made through a data bus 209 and a data bus 210.

[0063] Rearrangement of an above-mentioned indicative data has composition performed in connection with storing of the indicative data to this memory 207 (or 208), and read-out.

[0064] The bus selector 211 is for choosing either of the memory 207,208 and writing in an indicative data 107. Moreover, either memory 207 or the memory 208 is chosen, the indicative data stored in the selected memory concerned is read, and it outputs to a latch circuit 213 as an indicative data 212.

[0065] When the bus control signal 206 is "yes", the bus selector 211 changes the output bus 212 and a data bus 210 into a connection condition for the display data bus 107 and a data bus 209 again. On the other hand, when the bus control signal 206 is 'low", the output bus 212 and a data bus 209 are connected for the display data bus 107 and a data bus 210 again.

[0066] A latch circuit 213 stores an indicative data 212 temporarily according to the latch clock 214. The latch circuit 213 has composition outputted to the column circuit 110 by making the this memorized data into the indicative-data signal 126 after this.

[0067] The "selection electrical-potential-difference terminal", the "non-choosing electrical-potential-difference terminal", and the "gradation electrical-potential-difference terminal" which are said in a claim are equivalent to the terminal with which a power circuit 109 outputs a selection electrical potential difference, a non-choosing electrical potential difference, and a gradation electrical potential difference and the signal line connected to this, and a bus in this example. "X electrode switching means" is equivalent to the switch groups 118-121. Moreover, the group who divided X electrode is specified by whether it connects with which switch group.

[0068] The "1st memory" and the "2nd memory" are equivalent to memory 207 and memory 208 in this example. "A write-in means" and a "read-out means" are realized in the bus which connects the clock control section 201, the memory control section 202, the bus selector 211, and these cooperating closely, and operating. The "control means" whose "selection directions means" is a thing equivalent to a clock 201 is realized in the memory control section 202, the clock control section 201, and the bus selector 211 cooperating and operating.

[0069] Actuation of the liquid crystal display of this example is explained.

[0070] First, actuation of the display controller 102 and the column circuit 110 is explained using drawing 2 thru/or drawing 5 . Here, the case where the indicative data stored in memory 208 is read in parallel to this is explained, writing the indicative data 107 inputted from the outside in memory 207.

[0071] The blank signal 105 is set to the low level which means "it is effective." Then, the memory control circuit 203 makes the bus control signal 206 "yes." Moreover, while it can come, simultaneously the memory control section 203 "confirms" the write enable signal in the memory control signal 204, the

address which stores the data concerned is specified.
[0072] Then, the bus selector 211 outputs an indicative data 107 to memory 207 because the bus control signal 206 became "yes." In response, memory 207 stores the indicative data concerned in the address specified in the memory control signal 204.
[0073] In this case, if the data which it is going to write in are the first data (0th data), the memory control circuit 203 will specify address"0." The address 80 is specified to the following data (1st data). Furthermore, to the 2nd data inputted into this degree, the address 240 is specified for the address 160 to the 3rd data. The 4th data specify the address 1. To the 5th data, the address 241 is specified [the address 81] for the address 161 to the 7th data to the 6th data. That is, after shifting each group's start address 80 or more, the address is incremented one time every [1] in each groove.
[0074] By addressing in this way, the data outputted to X electrode through the 1st switch group 118 will be stored in the field from the address 0 to the address 79 as shown in drawing 5 R> 5. Moreover, the data outputted through the 2nd switch group 119 will be stored in the field to the addresses 80-159. Similarly, in the addresses 160-239, the data corresponding to the 4th switch group 121 in the data corresponding to the 3rd switch group 120 are stored in the addresses 240-319 again.
[0075] In parallel to write-in actuation of the indicative data to the memory 207 described above, the output to the latch circuit 213 of the data stored in memory 208 is also performed.
[0076] In drawing 3 , if Horizontal Synchronizing signal 104 becomes "effective", the clock control section 201 will output 80 read-out clocks in the memory control signal 202 (not shown) at a time.
[0077] Moreover, the memory control section 203 specifies the address which reads data in the memory control signal 205 synchronizing with this read-out clock. Sequential increment of the assignment of the address in this case shall be carried out every [1] from the address 0.
[0078] Then, the indicative data corresponding to the 1st switch group 118 is outputted to the beginning through the bus selector 211 to a latch circuit 213 from memory 208. Then, the sequential output of the data corresponding to the 2nd switch group 119, the 3rd switch group 120, and the 4th switch group 121 is carried out.
[0079] A latch circuit 213 memorizes the outputted data synchronizing with the latch clock 214. A latch circuit 213 continues outputting the latched data to the display data bus 126 until the following latch clock 214 becomes effective.
[0080] After outputting 80 read-out clocks, the clock control section 201 "confirms" the output clock contained in the column control signal 115. In addition, this output clock is for directing the timing which outputs a gradation electrical potential difference to the column circuit 110. Moreover, in the clock control section 201, in parallel to this, other switch groups turn ON at OFF the switch group to which the data currently outputted as an indicative data 126 correspond then with the switch control signals 122-125 again. For example, if the indicative data 126 at that time is a thing (it sets to drawing 5 and they are the addresses 80-159) corresponding to the 1st switch group 118, the 1st switch group 118 will be turned ON and the 2nd, 3rd, and 4th switch group 119,120,121 will be turned OFF. By this, the column circuit 110 will output the gradation electrical potential difference corresponding to the indicative-data signal 126 at that time only to a period until the following output clock becomes effective, and predetermined X electrode. In addition, since the column circuit 110 finishes outputting the gradation electrical potential difference corresponding to a front indicative data, the timing of the output of the switch control signals 122-125 will not be especially limited, if it is until it starts the output of the gradation electrical potential difference of the next **********. It does not matter even if it is after starting the output of the gradation electrical potential difference of an indicative data made into the purpose depending on the case. What is necessary is suitably, just to set up in accordance with the property of an actual each part circuit etc.
[0081] While the gradation electrical potential difference is impressed to X electrode (electrodes x0, x4, x8, --, x316) through the 1st switch group 118, the data (it sets to drawing 5 and they are the addresses 80-159) corresponding to the 2nd switch group 119 are read from memory 208. After this,

similarly, while the gradation electrical potential difference is outputted through the 2nd switch group 119 Data corresponding to the 3rd switch group 120 (in drawing 5) While the gradation electrical potential difference is further outputted for read-out of the addresses 160-239 through this 3rd switch group 120, read-out of the data (it sets to drawing 5 and them are the addresses 240-319) corresponding to the 4th switch group 121 is performed. The 4th control signal 125 is made into an invalid before the common circuit 112 chooses the following Y electrode. Thus, the writing to the memory 207 of an indicative data 107 and the output of the indicative data 126 from memory 208 finish by one line.

[0082] Then, if following Horizontal Synchronizing signal 104 becomes effective, an indicative data 107 will be shortly written in memory 208. And the indicative data of the following line is read from memory 207. Thus, by repeating read-out / write-in actuation by turns between memory 207,208, from the display controller 102, it is late for an indicative data 107 during 1 level period, and the indicative data 126 is outputted.

[0083] By repeating the above actuation, the gradient electrical potential difference corresponding to an indicative data is outputted to a liquid crystal panel 101 one by one.

[0084] Next, actuation of the common circuit 112 is explained using drawing 1 and drawing 6 .

[0085] If the Rhine signal which directs the change of the first line marker (it abbreviates to "FLM" hereafter) which shows the first Rhine among the common control signals 117, and selection Rhine like drawing 6 becomes effective, the common circuit 112 will output a selection electrical potential difference to an electrode y0 through the output bus 116. On the other hand, a non-choosing electrical potential difference is outputted to other Y electrodes (here electrodes y1-y239). Then, only the switching element of an electrode y0 will be in switch-on. Consequently, the gradation electrical potential difference currently then impressed to X electrode is impressed only to the pixel of the line corresponding to an electrode y0.

[0086] If the Rhine signal becomes effective next time, the common circuit 112 will output a selection electrical potential difference to an electrode y1 shortly. A non-choosing electrical potential difference is outputted to an electrode y0 and electrodes y1-y239. Thereby, the gradation electrical potential difference currently then impressed to X electrode is impressed only to the pixel of the line corresponding to an electrode y1. The display for one screen completes this actuation because even an electrode y239 repeats. Then, the display controller 102 confirms FLM and outputs a sequential selection electrical potential difference from an electrode y0 again.

[0087] As mentioned above, it enables the liquid crystal display of this example to perform the display corresponding to an indicative data by repeating the described actuation.

[0088] The 2nd example of this invention is explained using drawing 10 from drawing 7 .

[0089] The points performed by the input of the indicative data to a display controller and the output of this example of the indicative data from a display controller being parallel differ in an example 1. In addition, the following explanation may be given focusing on difference with an example 1, and explanation may be omitted about the same functional division.

[0090] An outline is explained first.

[0091] the column circuit 704 for driving X electrode of a liquid crystal panel 701 and a liquid crystal panel 701 as the liquid crystal display of this example is shown in drawing 7 , the common circuit 112 for driving Y electrode of a liquid crystal panel 701, the display controller 702 that operates the column circuit 704 and the common circuit 112 according to the indicative data inputted from the outside, and a power circuit 109 -- since -- it is constituted. Moreover, between the column circuit 704 and X electrode of a liquid crystal panel 701, it has the same configuration as the switch groups 118-121 in an example 1, and the switch groups 707-710 are formed in it. Naturally, these and below-mentioned each part are connected by the signal line for delivering and receiving various signals etc., and the bus.

[0092] A liquid crystal panel 701 is the thing of the active-matrix mold of 960 pixel x240 line.

[0093] Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105, the

dot clock 106, and the indicative data 703 are inputted into the display controller 702. The display controller 702 is generating and outputting the alternating current-ized signal 108, the column control signal 115, the common control signal 117, an indicative data 705, and the switch control signals 122-125 that control the switch groups 707-710 based on these inputs.

[0094] Synchronizing with a dot clock 106, as for the indicative data 703 in this example, 3 pixels is transmitted to coincidence (parallel). The display controller 702 rearranges this indicative data 703 into the sequence corresponding to each switch groups 707-710, and is outputting it to the column circuit 110 by making this into an indicative data 705. 3 pixels is sent to coincidence also for the indicative data 705 at parallel. Naturally the display data bus 703,705 is a thing corresponding to this.

[0095] The column circuit 704 memorizes an indicative data 705, is outputting the gradation electrical potential difference corresponding to the this memorized indicative data from the output bus 706 synchronizing with the output clock in the column control signal bus 115, and makes the display to a liquid crystal panel 701 perform. The column circuit 704 of this example can memorize the indicative data 705 to which the amount of 3 pixels collect into, and it is sent at a time. Since the column circuit 704 is equipped with the output of 240 pieces, this column circuit 704 is repeating this storage actuation 80 times, and it has memorized the indicative data for 240 outputs.

[0096] About the common circuit 112 and a power circuit 109, since it is the same as that of an example 1, explanation is omitted.

[0097] Next, the display controller 702 is further explained to a detail using drawing 8 R> 8.

[0098] The display controller 702 is constituted including the output bus 812 of the data bus 809,810 of memory 807 and 808 and memory 807,808 with which the clock control section 201, the memory control section 801, the latch clock bus 802, the data latch circuit 803, a bus 804, the memory control signal bus 805,806, and each can memorize the indicative data for one line, the bus selector 811, and the bus selector 812, the data latch circuit 813, and the bus control signal line 206 as shown in drawing 8 .

[0099] The memory control section 801 is generating the latch clock 802 and the memory control signals 805 and 806 based on the memory system control signal 202 supplied from the clock control section 201. And it passes through the latch clock 802 data latch circuit 803, and it is outputting the memory control signal 805,806 to memory 807,808. The latch clock 802 specifies the timing of incorporation of the indicative data 705 based on the data latch circuit 803, and the signal which synchronized with the dot clock 106 is included. The memory control signals 805 and 806 are constituted including the signal for specifying and changing the operating state (read-out/writing) of memory 807 and 808, respectively, the clock for specifying the timing of read-out/writing, and the address that performs read-out/writing.

[0100] The data latch circuit 803 is for rearranging the indicative data 703 inputted by parallel every 3 pixels corresponding to the switch groups 707-710. This data latch circuit 803 is outputting the indicative data after standing in a line and changing from the output bus 804. The data latch circuit 803 is further explained to a detail using drawing 9 after this. The "conversion means" said in a claim is equivalent to this data latch circuit 803 in this example.

[0101] Memory 807,808 can store the indicative data for one line, respectively. The operating state (writing/readout) is changed by the memory control signal 805,806 into which this memory 807,808 is inputted from the memory control section 801. Moreover, I/O of an indicative data is performed through a data bus 809,810.

[0102] Storing of the indicative data 804 to memory 807,808 is performed synchronizing with the clock in the memory control signal 805,806. Moreover, read-out of the indicative data from memory 807,808 has composition performed synchronizing with the read-out clock of the memory control signal 805,806.

[0103] The bus selector 811 is for changing the connection relation between the output bus 804, the output bus 812, a data bus 809, a data bus 810, and ** according to the bus control signal 206. That is, in reading an indicative data from memory 808 while an indicative data 804 is stored in memory 807, it connects the output bus 812 and a data bus 810 for the output bus 804 and a data bus 809 again. On

the contrary, from memory 807, while an indicative data 804 is stored in memory 808, in reading an indicative data, it connects the output bus 8112 and a data bus 809 for the output bus 804 and a data bus 810 again.

[0104] A latch circuit 813 latches the indicative data read from memory 807 (or 808) through the output bus 812, and outputs it as an indicative data 705. The latch is performed according to the latch clock 214. The output of an indicative data 705 is performed synchronizing with the data transfer clock contained in the column circuit control signal 115.

[0105] The data latch circuit 803 is further explained to a detail using drawing 9 .

[0106] The data latch circuit 803 consists of latch circuits 901-904, latch circuits 910-913, output buses 905-908, output buses 914-917, and a data selector 918.

[0107] Latch circuits 901-904 and latch circuits 910-913 can latch the indicative data for 3 pixels at a time. Each output bus 905-908 and the output buses 914-917 to an output of the latched data is possible for these.

[0108] The data selector circuit 918 chooses a predetermined thing out of the indicative data outputted through the output buses 914-917, and outputs it by making this into an indicative data 804 synchronizing with the latch clock 802. This selection is performed in sequence from which an indicative data 804 becomes a thing corresponding to the switch groups 707-710. The sequence of this selection is specified in fact with the latch clock 802 which the memory control section 801 outputs. The detail of this assignment is performed in explanation of operation.

[0109] Actuation of this example is explained using drawing 7 - drawing 10 . Explanation here is given centering on the display controller 702.

[0110] In drawing 8 , an indicative data 703 is sent to the display controller 702 synchronizing with a dot clock 106. Then, the data latch circuit 803 latches the indicative data for 4 times, i.e., 12 (3x4) pixel, for an indicative data 703 according to the latch clock bus 802. Furthermore, the indicative data for latched 12 pixels is rearranged into the sequence corresponding to the switch groups 707-710, and the data latch circuit 803 outputs it as an indicative data 804.

[0111] Every 3 pixels of indicative datas to which this indicative data 804 belongs to one certain switch group are gathered. That is, the 3-pixel partial output only of the data corresponding to the 1st switch group 707 is carried out to the beginning. Then, the 3-pixel partial output only of the data corresponding to the 2nd switch group 708 is carried out. After this, only every 3 pixels only of data corresponding to the 3rd switch group and the 4th switch group are outputted similarly, respectively. In addition, actuation of the data latch circuit 803 is further explained to a detail after this using drawing 9 and drawing 10 .

[0112] This indicative data 804 is stored in either among memory 807 and memory 808. If the bus control signal 206 is a "low", the bus selector 811 makes switch-on the output bus 804 and the output bus 809. Therefore, the indicative data 804 outputted from the data latch circuit 803 at this time is written in memory 807. When the bus control signal 206 is "yes", the indicative data 804 outputted at this time is written in memory 808.

[0113] Corresponding to each switch groups 707-710, the memory control section 801 specifies the address which writes in data. For example, since the first data for 3 pixels are a thing corresponding to the 1st switch group 707, they specify the address 0. Since the continuing data for 3 pixels are a thing corresponding to the 2nd switch group 708, they specify the address 80. The address 240 is specified as the data corresponding to the 4th switch group 710 for the address 160 at the continuing data corresponding to the 3rd switch group 709. Since the liquid crystal panel of this example is equipped with 960 X electrodes, the initial value of the address assigned to each switch group needs to open or more 80 spacing.

[0114] In addition, in drawing 10 , the memory control section 801 confirms the write enable signal of the memory control signal 805 synchronizing with falling of 5 clock eye of a dot clock 106, after the blank signal 105 becomes effective. And it synchronizes with a dot clock 106 henceforth, and it is the condition (effective (low)/invalid (yes) is controlled.) of a write enable signal. By drawing 10 , the

indicative data 804 was written in memory 807, and the situation in case read-out actuation described below to memory 808 is performed was shown.
[0115] In parallel to the above storing actuation, read-out of the indicative data from memory 808 and the transfer to the column circuit 704 are performed.
[0116] The address of the data to read is specified by the memory control signal 806 inputted from the memory control section 801. If Horizontal Synchronizing signal 104 becomes effective, the memory control section 801 will carry out sequential increment of the this specified address from 0 to 79 synchronizing with the read-out clock in the memory system control signal 202. The mask of this read-out clock is carried out after 80 clock output. The read data are outputted to the data latch circuit 813 through the output bus 810, the bus selector 811, and the output bus 812.
[0117] The data latch circuit 813 latches this indicative data 812 according to the latch clock 214. Then, this is outputted to the column circuit 704 as an indicative data 705 synchronizing with the data transfer clock in the column circuit control signal 115.
[0118] The column circuit 704 carries out the sequential storage of the indicative data 705. And if the output clock of the column control signal bus 115 becomes effective, a gradation electrical potential difference will be outputted to the output bus 706.
[0119] After an output clock becomes effective, a read-out clock becomes "effective" by 80 clocks again. The memory control section 801 makes the indicative data from address "80" to "159" read from memory 808 at this time. After this, the same processing is repeated.
[0120] By repeating the above read-out actuation, the gradation electrical potential difference corresponding to the indicative data for one line stored in memory 808 can be outputted.
[0121] Next, actuation of the data latch circuit 803 is further explained to a detail using drawing 9 and drawing 10 .
[0122] Here, in order to clarify the location displayed on a liquid crystal panel 701, it is made ****** which gives a number called n-m to an indicative data. When n divides 960 X electrodes (an electrode x0 - electrode x959) every four sequentially from left-hand side, the field where the electrode with which the indicative data concerned is outputted belongs is the number which shows the field of what position it is from left-hand side. m is a number which shows in what position the electrode with which the indicative data concerned is outputted is located from left-hand side in the field. However, m shall begin from n and0. The location in the inside of the whole X electrode of the electrode with which a certain indicative-data n-m is outputted can be expressed with 3 n+m. In other words, indicative-data n-m is data outputted to Electrode x (3 n+m). For example, an indicative data 0-0 is an indicative data of the electrode x0 of a liquid crystal panel 701. An indicative data 0-1 should be outputted to an electrode x1, and an indicative data 0-2 should be outputted to electrode x2.
[0123] As for each part of the data latch circuit 803, the timing of operation is determined according to the latch clock 802. Five kinds of latch clocks (each is hereafter called "1st latch clock "-" 5th latch clock") are contained in this latch clock 802.
[0124] The 1st - the 4th latch clock are confirmed for every four cycle of a dot clock 106 as shown in drawing 10 . In an order from the 1st clock, these are behind in the one-cycle [every] phase of a dot clock 106. The 5th latch clock is made effective [once] for every four cycle of dot KURO@KKU 106. This 5th latch clock is behind the 4th latch clock in the phase by the half cycle of a dot clock 106.
[0125] In drawing 10 , if the blank signal 105 becomes effective, synchronizing with falling of the beginning of a dot clock 106, the 1st latch clock will become effective. Then, a latch circuit 901 latches the indicative data 0-0 of the indicative datas 703 - an indicative data 0-2 synchronizing with this. this -- then, a latch circuit 902 - a latch circuit 904 latch the indicative data for 12 pixels to an indicative data 1-0 to 3-2 similarly synchronizing with the 2nd latch clock - 4th latch clock.
[0126] Latch circuits 901-904 output this latched indicative data at a time at latch circuits 910-914 synchronizing with the 5th latch clock. Outputting latch circuits 910-914 is continued from the output buses 914-917 until it latches this and the 5th latch clock becomes "effective" next time.

[0127] A data selector 918 chooses from latch circuits 901-904 only the indicative-data train (1 here the electrodes x0, x4, and x the indicative data 0-0, 1- which corresponded eight times two -2) corresponding to the 1st switch group 707 among the data for 12 pixels outputted to coincidence, and outputs it to the bus selector 811 by making this into an indicative data 804. The output in this case is performed synchronizing with the next 1st latch clock.
[0128] Then, a data selector 918 chooses only the indicative-data train corresponding to the 2nd switch group 708, and outputs it to the bus selector 811 by making this into an indicative data 804. The output in this case is performed synchronizing with the 2nd latch clock. A data selector 918 outputs the indicative data corresponding to the 4th switch group 710 for the indicative data corresponding to the 3rd switch group 709 as an indicative data 804 like the following synchronizing with the 4th latch clock synchronizing with the 3rd latch clock.
[0129] According to the 2nd example explained above, it is parallel, and it can respond to highly minute-ization of a liquid crystal panel, without changing column circuit 704 grade also to the indicative data inputted.
[0130] The 3rd example of this invention is explained.
[0131] As for this 3rd example, an asynchronous point differs [the data reading clock from memory, and the data write-in clock to memory] from the 2nd example mutually.
[0132] The liquid crystal display of this example is constituted including a liquid crystal panel 701, the column circuit 704 for driving X electrode of a liquid crystal panel 701, the common circuit 112 for driving Y electrode of a liquid crystal panel 701, the display controller 1101 that operates the column circuit 704 and the common circuit 112 according to the indicative data inputted from the outside, a power circuit 109, and the switch groups 707-710 as shown in drawing 11 . Furthermore, the display controller 1101 is equipped with the oscillator 1102 which supplies an external clock 1103 in this example. This external clock 1103 is made into the radical of the read-out clock of the indicative data from memory as it is mentioned later.
[0133] The external clock 1103 into which the display controller 1101 is inputted from an oscillator 1102 in addition to the various input signals 103,104,105,106 and an indicative data 703 is inputted as already stated. Based on these inputs, the display controller 1102 generates an indicative data 705 and the various signals 115,122 - 125,108,117 grades, and is outputting them synchronizing with an external clock 1103.
[0134] The detail of the display controller 1101 is explained using drawing 12 .
[0135] The display controller 1101 is constituted including the clock control section 1201, the clock control section 1203, the memory control section 1205, the bus selector 1208, memory 1213 and 1214, the data latch circuit 803, and the data latch circuit 813 as shown in drawing 12 . Moreover, between these each part was connected and it has the various buses for performing transfer of data and a signal, and a signal line. In addition, in order to simplify drawing, in drawing 12 , the signals 115,122-125,108,117 in drawing 11 are packed, and it is drawing as a signal 1126.
[0136] The clock control section 1201 generates the write-in control signal 1202 and the latch clock 802 based on Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, the blank signal 105, and dot KURO@KKU 106.
[0137] Vertical Synchronizing signal 103, Horizontal Synchronizing signal 104, and the write-in clock are contained in the write-in control signal 1202. Vertical Synchronizing signal 103 and Horizontal Synchronizing signal 104 are used in order that the memory control section 1205 may judge the data of how many lines an indicative data 804 is. A write-in clock is for an indicative data 804 to tell the memory control section 1205 about the effective time amount range.
[0138] The clock control section 1203 generates the memory reading control signal 1204 which synchronized with the external clock 1103, a signal 1216, and the latch clock 214.
[0139] The memory control section 1205 controls the writing of the data to memory 1213 and 1214, and read-out of the data from these. This memory control section 1205 has composition which generates

the memory write-in control signal 1206 which synchronized with the dot clock 106, the memory reading control signal 1207 which synchronized with the external clock 1103, and the bus control signal 206 based on the write-in control signal 1202 and the reading control signal 1204, and outputs this to a selector 1208.

[0140] The memory write-in control signal 1206 and the memory reading control signal 1207 consist of the lead enable signal, a write enable signal, an address signal, and a data signal, respectively (refer to drawing 13). A read-out enable signal is to show read-out completion. In addition, the bus control signal 206 and the lead enable signal are outputted also to the clock control section 1203 through the bus 1204.

[0141] The data latch circuit 803 and the data latch circuit 813 have the same function as an example 2.

[0142] Memory 1213 and 1214 is equipped with the capacity which can memorize the indicative data for ******** 1 screen. The method of arrangement of the indicative data within memory 1213 and 1214 is the same as that of examples 1 and 2 fundamentally (refer to drawing 5). However, in this example, it is what has arranged the data of each Rhine side by side by the number of the scanning line of a liquid crystal panel (this example 240 duties) as it is shown in drawing 14 , in order to memorize data by one screen. Arrangement of such data is realized by the method of assignment of the address from the memory control section 1205.

[0143] The bus selector 1208 changes the connection relation between a bus 804, a bus 1215, and a bus 1211 and a bus 1212 according to the bus control signal 206. Moreover, the connection relation between the write-in control signal bus 1206, the read-out control signal bus 1207, and the memory control buses 1209 and 1210 is changed.

[0144] When the bus control signal 206 of this bus selector 1208 is "yes", an indicative data 804 is written in memory 1213, and read-out of an indicative data is made to be performed from memory 1214. That is, it writes in with the memory control bus 1209, and let the output bus 8804 and a data bus 1211 be switch-on for the control signal bus 1206 again. Furthermore, let the memory control bus 1210 and the memory-write-signals bus 1207 be switch-on for the output bus 1215 and the memory data bus 1212 again.

[0145] On the other hand, when the bus control signal 206 is a "low", an indicative data 804 is written in memory 1214, and read-out of an indicative data is made to be performed from memory 1213. That is, it writes in with the memory control bus 1210, and let the output bus 804 and a data bus 1212 be switch-on for the control signal bus 1206 again. Furthermore, let the memory control bus 1209 and the memory-write-signals bus 1207 be switch-on for the output bus 1215 and the memory data bus 1211 again.

[0146] Actuation of this example is explained using drawing 13 .

[0147] In drawing 11 , actuation of this example is the same as that of an example 2 except the alternating current-ized signal 108, the column control signal bus 115, the common control signal bus 117, the 1st control signal 122, the 2nd control signal 123, the 3rd control signal 124, the 4th control signal 125, and an indicative data 705 being outputted synchronizing with an external clock 1103. Therefore, only the interior action of the display controller 1101 is explained here.

[0148] The clock control sections 1201 and 1203 are outputting the various signals 802, 1202, 11204, 214, and 1216 based on the signals 103, 104, 105, 106, and 1103 inputted from the outside.

[0149] Moreover, the memory control section 1205 reads with the write-in control signal 1202, from the control signal 1204, generates the memory write-in control signal 1206 and the memory reading control signal 1207, and is outputting them to the selector 1208. Moreover, the bus control signal 206 is outputted to the selector 1208.

[0150] The data latch circuit 803 incorporates an indicative data 703 synchronizing with the latch clock 802 inputted from the clock control section 1201, and after putting in order and changing this, it outputs it as an indicative data 804 corresponding to each switch groups 707-710. The detail of this rearrangement is the same as an example 2. The data for 3 pixels corresponding to one certain switch

group are outputted as an indicative data 804 one by one for every switch group.
[0151] The memory control section 1205 makes the indicative data 804 for one screen store in either of memory 1213 and memory 1214 by the selector 1208. Moreover, the indicative data for one screen is made to read from memory 1213 (or 1214), being outputted from the clock control section 1203, reading in parallel to this, and synchronizing with a clock. Read-out of this indicative data is performed like other examples from the memory of the direction where write-in actuation of data is not then performed.
[0152] The data latch circuit 813 latches the indicative data read from memory 1213 (or 1214) synchronizing with the latch clock 214. And synchronizing with the transfer clock contained in the column control signal 115 (drawing 12 signal 1216), an indicative data is outputted as an indicative data 705.
[0153] If read-out is completed, the memory control section 1205 will make the lead enable signal in the memory control signal 1207 an invalid (this example "low"), as shown in drawing 13 . The clock control section 1203 which received this lead enable signal stops the output of a read-out clock.
[0154] The memory control section 1205 changes the condition (yes, /low) of the bus control signal 206 as it is shown in drawing 13 , when read-out from storing in memory 1213 and memory 1214 of the indicative data for one screen is completed.
[0155] Then, a selector 1208 will operate corresponding to this and the memory in which an indicative data 804 is stored, and the memory from which an indicative data is read will interchange next time. Moreover, the clock control section 1203 initializes oneself corresponding to the status change of the bus control signal 206. And it prepares for the display of degree screen and generation of a signal 1216 is begun again. Furthermore, the clock control section 1203 resumes the output to the memory control section 1205 of a read-out clock. The memory control section 1205 which received this read-out clock reads an indicative data from address "0" one by one synchronizing with this read-out clock.
[0156] being possible in the display to a liquid crystal panel 701, though the liquid crystal display of this example has two asynchronous clocks by repeating the above actuation -- ** -- it is carrying out.
[0157] The 4th example is explained.
[0158] This 4th example arranges the switch group which chooses the output of a common circuit between a common circuit and Y electrode of a liquid crystal panel, and the points which control this by the display controller differ in the example 1. About other points, it is the same as that of an example 1 fundamentally. It is applied when this example has few outputs of a common circuit than the number of Rhine of a liquid crystal panel.
[0159] The liquid crystal display of this example is explained using drawing 15 .
[0160] Liquid crystal panel 101 the very thing is the same as that of an example 1. However, Y electrode which it has 240 is divided into two groups, and impression of its selection / non-choosing electrical potential difference is controlled by this example. Hereafter, Y electrode located in the field of a lower half on the other hand with the 1st common bus 1610 in Y electrode located in the field of the upper half in drawing 15 is called the 2nd common bus 1611.
[0161] The switch groups 1606-1609 are for changing the connection relation between Y electrode of a liquid crystal panel, the output bus 1604 of the common circuit 1603, and the non-choosing electrical-potential-difference signal line 1605 from a power circuit 109.
[0162] The non-choosing electrical potential difference which a power circuit 109 generates is outputted even if it leads the non-choosing electrical-potential-difference signal line 1605 which branched and has come out of the middle of the scan electrical-potential-difference bus 113. This non-choosing electrical-potential-difference signal line 1605 is constituted possible [the 2nd common bus 1611 and connection] through the 4th switch group 1609 with the 1st common bus 1610 of a liquid crystal panel again through the above-mentioned 2nd switch group 1607.
[0163] Otherwise, the common circuit 1603 outputs a non-choosing electrical potential difference for a selection electrical potential difference to either among the output terminals y0-y119 which constitute the output bus 1604. It is directed by the common control signal 1602 inputted from the display

controller 1601 whether to output a selection electrical potential difference from which output terminal.
[0164] The output bus 1604 of the common circuit 1603 of this example is connectable with the 2nd common bus 1611 through the 1st common bus 1610 and the 3rd switch group 1608 through the 1st switch group 1606.
[0165] The display controller 1601 is generating and outputting the common control signal 1602 for controlling the common circuit 1603. Furthermore, it has composition which outputs the 1st control signal 1612 for controlling the switch groups 1606–1609, and the 2nd control signal 1613. The clock control section 201 of drawing 2 is generating these control signals 1612 and 1613. The internal configuration of the display controller 1601 is the same as that of drawing 2 fundamentally. Naturally, the 1st control signal 122 for controlling the switch groups 118–121 – the 4th control signal 125 are also outputted.
[0166] The 1st switch group 1606 and the 4th switch group 1609 are turned ON, and, on the other hand, the display controller 1601 turns OFF the 2nd switch group 1607 and the 3rd switch group 1608, when impressing a selection electrical potential difference to either of the Y electrodes belonging to the 1st common bus 1610. Thereby, the output from the common circuit 1603 is impressed to the 1st common bus 1610, and the non-choosing voltage signal 1605 is impressed to the 2nd common bus 1611. On the contrary, in impressing a selection electrical potential difference to either of the Y electrodes belonging to the 2nd common bus 1611, the 1st switch group 1606 and the 4th switch group 1609 are turned OFF, and, on the other hand, it turns ON the 2nd switch group 1607 and the 3rd switch group 1608. Thereby, the non-choosing voltage signal 1605 is impressed to the 1st common bus 1610, and the output from the common circuit 1603 is impressed to the 2nd common bus 1611.
[0167] "Y electrode switching means" said in a claim is realized by the switch groups 1606–1609. The "group" of Y electrode is equivalent to the 1st common bus 1610 and the 2nd common bus 1611.
[0168] Actuation of this example is explained using drawing 15 and drawing 16 .
[0169] Actuation of this example is fundamentally the same as the 1st example of the above except actuation of the common circuit 1603. Therefore, only actuation of the common circuit 1603 is explained here.
[0170] "during the period which should choose either of the Y electrodes belonging to the 1st common bus 1610, and the display controller 1601 -- the 1st control signal 1612 -- it is effective" [(yes)] -- moreover, let the 2nd control signal 1613 be an "invalid" (low). Consequently, the 1st switch group 1606 and the 4th switch group 1609 are turned on (switch-on), and, on the other hand, the 2nd switch group 1607 and the 3rd switch group 1608 are turned off (cut off state). In this condition, the non-choosing electrical potential difference 1605 will be impressed to Y electrode with which the selection / non-choosing electrical potential difference 1604 which the common circuit 1603 outputs to Y electrode belonging to the 1st common bus 1610 belong to the 2nd common bus 1611 on the other hand. The common circuit 1603 synchronizes with the Rhine signal the output terminal which outputs a selection electrical potential difference in the meantime, and is y0->y1->y2-> one by one... It is changing with ->y199 and is scanning within the limits of the 1st common bus 1610.
[0171] the "display controller 1601 after the scan to Y electrode (electrodes y0–y119) belonging to the 1st common bus 1610 finishes (that is, after choosing an electrode y199) -- next time -- the 2nd control signal 1613 -- it is effective" [(yes)] -- moreover, let the 1st control signal 1612 be an "invalid" (low). Consequently, the 1st switch group 1606 and the 4th switch group 1609 are turned off (cut off state), and, on the other hand, the 2nd switch group 1607 and the 3rd switch group 1608 are turned on (switch-on). In this condition, the selection / non-choosing electrical potential difference 1604 which the common circuit 1603 outputs will be impressed to Y electrode with which the non-choosing electrical potential difference 1605 belongs to the 2nd common bus 1611 on the other hand at Y electrode belonging to the 1st common bus 1610. Consequently, Y electrode with which the selection electrical potential difference which the common circuit 1603 outputs is impressed is y120->y121->y122->... It will be changed one by one with ->y239.

[0172] In addition, based on the timing of FLM and the Rhine signal, effective (yes) is performed and the display controller 1601 is making an invalid (low) change of the 1st control signal 1612 and the 2nd control signal 1613. In the example shown in drawing 16 , the common circuit 1603 outputs a selection electrical potential difference to an output terminal y0 ignited by the Rhine signal becoming effective during the period when the FLM signal in the common control signal 1602 has become yes. It is a time of impressing a selection electrical potential difference to an electrode y120 that the common circuit 1603 outputs a selection electrical potential difference to an output terminal y0 next time, after the 120 clock partial output of the clock in the Rhine signal 1602 is carried out that is,.

[0173] In this example, even when there are few output buses of the common circuit 1603 than the number of Y electrodes of a liquid crystal panel, an electrode y0 to the electrode y239 of a liquid crystal panel can scan sequentially.

[0174] According to the 1st explained above - the 4th example, it can respond easily to highly minute-ization of a liquid crystal panel. Moreover, even when there is modification to which the number of pixels and the number of Rhine of a liquid crystal panel are made to increase, according to the increment, it can respond by making the storage capacity of memory increase.

[0175] When there are more effective datas of an indicative data than the number of displays of a liquid crystal panel, it is possible also for displaying on a liquid crystal panel only the field part as which it was beforehand determined of the display images. In order to realize this, the register which memorizes the coordinate value which shows the range of the image field displayed on a liquid crystal panel is prepared in a display controller. And what is necessary is to compare the display position of the inputted indicative data with the coordinate value stored in this register, and to memorize in memory only the indicative data about the image field specified in the register. If it does in this way, an aspect ratio can also display a different image from the liquid crystal panel.

[0176] In the above-mentioned example, although rearranged at the time of the writing to the memory of an indicative data, it reads conversely and may be made to sometimes rearrange. For example, an indicative data is put in order and stored in the order which usually passed and was inputted at the time of writing. And what is necessary is just to increment the address every [4] at the time of read-out, in case a series of indicative datas corresponding to one certain switch group are read. In case the data corresponding to the 1st switch group are read, the addresses 0 and 4 and 8 -- are specified.

[0177] At this example, the display controller has been miniaturized by making it one LSI.

[0178]

[Effect of the Invention] It can respond to highly minute-ization of a liquid crystal panel, without making small the output pitch of a common circuit and column circuit which is a liquid crystal drive circuit according to this invention.

[0179] Also when a write-in clock and a read-out clock are asynchronous clocks, it can respond by having the memory for one screen.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the liquid crystal display which is the 1st example of this invention.

[Drawing 2] It is the block diagram showing the internal configuration of the display controller 102.

[Drawing 3] It is the timing chart of data writing / read-out in memory 207,208.

[Drawing 4] It is the timing chart of control signals 122-125 which operates the switch groups 118-121.

[Drawing 5] It is the map in which the arrangement condition of the indicative data within memory 207,208 is shown.

[Drawing 6] It is the timing chart of the signal which controls the common circuit 112.

[Drawing 7] It is the whole liquid crystal display block diagram which is the 2nd example of this invention.

[Drawing 8] It is the block diagram showing the internal configuration of the display controller 702.

[Drawing 9] It is the block diagram showing the internal configuration of the data latch circuit 803.

[Drawing 10] It is the timing chart of storing / read-out actuation of the indicative data to memory 207,208.

[Drawing 11] It is the whole liquid crystal display block diagram which is the 3rd example of this invention.

[Drawing 12] It is the block diagram showing the internal configuration of the display controller 1101.

[Drawing 13] It is the timing chart of storing / read-out actuation of the indicative data to memory 1213 and 1214.

[Drawing 14] They are memory 121 and the memory map in which the situation of arrangement of the indicative data in 1214 is shown.

[Drawing 15] It is the whole liquid crystal display block diagram which is the 4th example of this invention.

[Drawing 16] It is the timing chart which shows the relation between the output voltage of the common circuit 1603, and the electrical potential difference impressed to y electrode.

[Drawing 17] It is the block diagram of the liquid crystal display of the conventional example.

[Drawing 18] It is the timing chart of the conventional example.

[Drawing 19] It is the block diagram of the column circuit HD 66310 of the conventional example.

[Description of Notations]

101 -- A liquid crystal panel, 102 -- A display controller, 103 -- Vertical Synchronizing signal, 104 -- Horizontal Synchronizing signal 105 -- A blank signal, 106 -- Dot clock, 107 [-- Column circuit,] -- A display data bus, 108 -- Alternating current-ized signal 109 -- A power circuit, 110 111 -- A gradient electrical-potential-difference bus, 112 -- A common circuit, 113 -- Scan electrical-potential-difference bus, 114 -- An output bus, 115 -- A column control signal bus, 116 -- Output bus, 117 -- Common control bus 118 -- The 1st switch group, 119 -- The 2nd switch group, 120 -- The 3rd switch group, 121 -- The 4th switch group, 122 -- The 1st control signal, 123 -- The 2nd control signal, 124 -- The 3rd control signal, 125 -- The 4th control signal, 126 -- A display data bus, 127 -- An opposite electrical-potential-difference line, 201 -- Clock control section, 202 -- A memory system control bus, 203 -- A memory control section, 204 -- Memory control bus, 205 -- A memory control bus, 206 -- A bus control signal, 207 -- Memory, 208 [-- Bus selector,] -- Memory, 209 -- A data bus, 210 -- A data bus, 211 212 -- An output bus, 213 -- A latch circuit, 214 -- Latch clock, 701 -- A liquid crystal panel, 702 -- A display controller, 703 -- Display data bus, 704 -- A column circuit, 705 -- A display data bus, 706 -- Output bus, 707 -- The 1st switch group, 708 -- The 2nd switch group, 709 -- The 3rd switch group, 710 -- The 4th switch group, 801 -- A memory control section, 802 -- Latch clock bus, 803 -- A data latch circuit, 804 -- An output bus, 805 -- Memory control signal bus, 806 [-- Data bus,] -- A memory control signal bus, 807 -- Memory, 808 -- Memory, 809 810 [-- Data latch circuit,] -- A data bus, 811 -- A bus selector, 812 -- An output bus, 813 901-904 -- A latch circuit,

905-908 -- An output bus, 910-913 -- Latch circuit, 914-917 -- An output bus, 918 -- A data selector circuit, 1101 -- Display controller, 1102 -- An oscillator, 1103 -- An external clock, 1201 -- Clock control section (1), 1202 -- A write-in control signal bus, 1203 -- Clock control section (2), 1204 -- A reading control signal bus, 1205 -- A memory control section, 1206 -- Memory-write-signals bus, 1207 -- A memory reading control signal bus, 1208 -- Bus selector, 1209 -- A memory control signal bus, 1210 -- A memory control signal bus, 1211 -- Memory data bus, 1212 -- A memory data bus, 1213 -- Memory, 1214 -- Memory, 1215 -- A data bus, 1216 -- A control signal bus, 2100 -- Column circuit, 2101 [-- Enable signal,] -- A signal line, 2103 -- A latch circuit, 2104 -- A clock, 2105 2110 -- A driver control means, 2111 -- A clock, 2120 -- Data-conversion circuit, 2121 -- A frequency divider, 2122 -- A delay circuit, 2130 -- Column circuit group, 2131 [-- A synchronizing signal, 2301 / -- A latch address counter, 2302 / -- A latch circuit, 2303 / -- A latch circuit, 2304 / -- A level-shifter circuit, 2305 / -- A liquid crystal drive circuit, 2306 / -- Liquid crystal driver voltage] -- A scan drive circuit, 2132 -- A liquid crystal panel, 2401 -- An indicative data, 2402

[Translation done.]

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最終頁に続く

(54)【発明の名称】　液晶表示装置

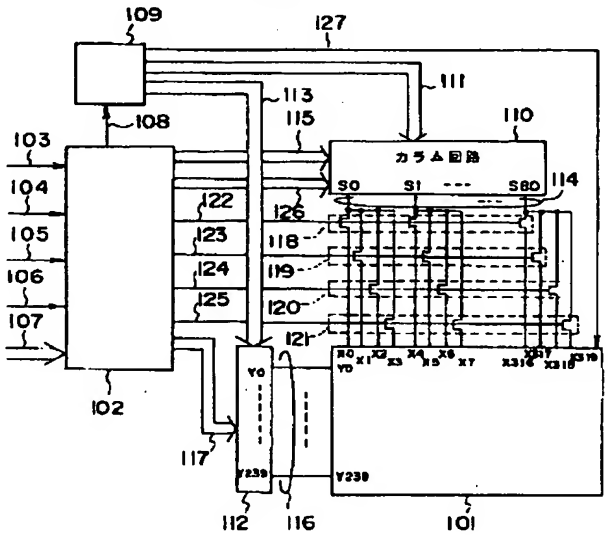
(57)【要約】

【目的】　従来の液晶駆動回路を用いて、画素ピッチを微細化した液晶パネルに良好な表示を行うことための表示コントローラを実現する。

【構成】　表示コントローラ１０２によって、スイッチ群１１８～１２１に対応して表示データを並べ替える。そして、各スイッチ群に対応するデータ毎に、順次、表示データ１２６をカラム回路１１０へ出力する。そして、出力する表示データ１２６に対応して、制御信号１２２～１２５によって、スイッチ群１１８～１２１を開閉させる。これにより、表示データを、当該表示データが対応するスイッチ群に接続されているＸ電極にのみ出力することができる。

【効果】　カラム回路の出力端子数の増大、出力端子ピッチの微細化を必要とすることなく、高精細の液晶パネルに対応できる。

図１



1

【特許請求の範囲】

【請求項１】Ｍ個のＹ電極と、Ｎ個のＸ電極とを備えた、アクティブマトリックス型の液晶パネルと、

選択電圧と、非選択電圧と、複数種類の階調電圧とを生成する機能を備え、上記選択電圧を出力する選択電圧端子と、上記非選択電圧を出力する非選択電圧端子と、上記階調電圧を出力する階調電圧端子とを備えた電源回路と、

ｎ個（ｎ＜Ｎ）の出力端子を備え、上記電源回路から出力される上記階調電圧のうちのいずれかを、別途与えられたデータ列に対応して該出力端子毎に選択し、該選択した階調電圧を当該出力端子から出力するカラム回路と、

上記Ｙ電極のいずれか一つに上記選択電圧を、また、その他のＹ電極には上記非選択電圧を印加するコモン手段と、

構成要素がｎ個以下である複数のグループに上記Ｘ電極を分類し、該グループのうちいずれか一つを選択して、該選択されたグループに属するＸ電極のみを上記カラム回路の上記出力端子と予め定められた対応関係をもって接続するＸ電極スイッチ手段と、

少なくとも、表示データと水平同期信号とが外部から入力されており、該外部から入力された表示データの順番を並べ替えて、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、上記カラム回路へ出力する表示コントローラと、

を有することを特徴とする液晶表示装置。

【請求項２】上記表示コントローラは、

少なくとも１ライン分のデータを記憶可能な第１のメモリと、

少なくとも１ライン分のデータを記憶可能な第２のメモリと、

外部から入力されてくる表示データを取り入れ、上記第１のメモリまたは第２のメモリに書き込む書き込み手段と、

上記第１のメモリと第２のメモリとのうち、その時点で上記書き込み手段による書き込み動作の実行対象となっていない方から、当該メモリに既に格納されている表示データを、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、読み出して出力する読み出し手段と、

上記カラム回路が、あるグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力を開始する前に、上記Ｘ電極スイッチ手段による上記グループの選択を、該次のグループのＸ電極とカラム回路の出力端子とが接続されるように変更させる選択指示手段と、

上記書き込み手段による上記表示データの書き込み動作の対象とされるメモリを、上記水平同期信号が有効になるのを契機として、上記第１のメモリと上記第２のメモリとの間で交互に切り替えさせる制御手段と、

を含んで構成されることを特徴とする液晶表示装置。

2

【請求項３】請求項１記載の液晶表示装置において、

上記表示データの外部からの入力はパラレルで行われるものであり、

上記外部から入力されてくる表示データを予め定められた画素数分だけ受け付けて、該受け付けた表示データを、当該表示データが対応するＸ電極の属するグループに基づいて分類して、該分類毎に出力する変換手段をさらに備え、

上記書き込み手段は上記変換手段が出力する表示データを、上記第１のメモリまたは上記第２のメモリに書き込むものであること、

を特徴とする液晶表示装置。

【請求項４】請求項１記載の液晶表示装置において、

上記書き込み手段は、別途生成される書き込みクロックに同期して、上記書き込み動作を行うものであり、

上記読み出し手段は、上記書き込みクロックとは非同期の別途生成される読み出しクロックに同期して、上記読み出しを行うものであり、

上記制御手段は、上記書き込み手段による上記表示データの書き込み対象とされるメモリの切り替えを、上記水平同期信号に代わって、１画面分の表示データを書き込んだことを確認して行わせるものであり、

上記第１のメモリおよび上記第２のメモリは、上記液晶パネル１画面分の表示データを記憶可能な記憶容量を備えること、

を特徴とする液晶表示装置。

【請求項５】請求項１記載の液晶表示装置において、

上記コモン手段は、

ｍ個（ｍ＜Ｍ）の出力端子を備え、該出力端子のうちの１つを順次選択し、該選択された出力端子からは上記選択電圧を、他の出力端子からは非選択電圧を出力するコモン回路と、

上記Ｙ電極を構成要素がｍ個以下である複数のグループに分け、いずれかのグループに属するＹ電極のみを選択的に上記コモン回路の上記出力端子と予め定められた対応関係をもって接続するとともに、その時点で上記コモン回路と接続されていないＹ電極を上記電源回路の非選択電圧端子に接続するＹ電極スイッチ手段と、を備え、

上記表示コントローラは、上記コモン回路がすべての出力端子を選択し終わる度ごとに、上記Ｙ電極スイッチ手段による上記グループの選択を変更させるものであること、

を特徴とする液晶表示装置。

【請求項６】請求項１記載の液晶表示装置において、

上記第１のメモリおよび上記第２のメモリは、その記憶容量を変更可能に構成されていること、

を特徴とする液晶表示装置。

【請求項７】Ｍ個のＹ電極と、Ｎ個のＸ電極とを備え

3

た、アクティブマトリックス型の液晶パネルと、
ｎ個（ｎ＜Ｎ）の出力端子を備え、該出力端子から別途別途与えられたデータ列に対応した階調電圧を出力するカラム回路と、
構成要素がｎ個以下である複数のグループに上記Ｘ電極を分類し、該グループのうちいずれか一つを選択して、該選択されたグループに属するＸ電極のみを上記カラム回路の上記出力端子と予め定められた対応関係をもって接続するＸ電極スイッチ手段と、
を含んで構成された液晶表示装置の駆動に使用される表示コントローラにおいて、
少なくとも１ライン分のデータを記憶可能な第１のメモリと、
少なくとも１ライン分のデータを記憶可能な第２のメモリと、
外部から入力されてくる表示データを取り入れ、上記第１のメモリまたは第２のメモリに書き込む書き込み手段と、
上記第１のメモリと第２のメモリとのうち、その時点で上記書き込み手段による書き込み動作の実行対象となっていない方から、当該メモリに既に格納されている表示データを、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、読み出して出力する読み出し手段と、
上記カラム回路が、あるグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力を開始する前に、上記Ｘ電極スイッチ手段による上記グループの選択を、該次のグループのＸ電極とカラム回路の出力端子とが接続されるように変更させる選択指示手段と、
上記書き込み手段による上記表示データの書き込み動作の対象とされるメモリを、上記水平同期信号が有効になるのを契機として、上記第１のメモリと上記第２のメモリとの間で交互に切り替えさせる制御手段と、
を含んで構成されることを特徴とする表示コントローラ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、パソコン、ワークステーション等の表示データを液晶パネルに表示させるのに好適な液晶表示コントローラに関する。

【０００２】

【従来の技術】パソコン、ワークステーション等では、液晶表示装置が広く使用されている。

【０００３】以下、液晶表示装置の構成及び動作を、図１７，１８，１９を用いて説明する。　ここでの説明は、水平解像度が、Ｒ，Ｇ，Ｂの各画素につき６４０画素（合計１９２０（＝６４０×３）画素）、垂直解像度が４８０ラインの液晶パネルを、株式会社日立製作所製の表示コントローラ（商品名”カラム回路ＨＤ６６３１０”）によって駆動する場合を例にとって行う。なお、該説明の内容については、株式会社日立製作所半導体事業部発行の日立ＬＣＤドライバＬＳＩデータブックｐ６６１、６６２に記載されているものである。

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【０００４】図１７に示すとおり、ドライバ制御手段２１１０には、表示データ２４０１と、これに同期した同期信号２４０２とが、パソコンやワークステーション等から入力されている。なお、同期信号２４０２には、ドットクロック、水平同期信号、垂直同期信号が含まれる。

【０００５】ドライバ制御手段２１１０内のデータ変換回路２１２０は、後述するカラム回路２１００のインタフェイスに合わせるように表示データ２４０１を変換している。そして、該変換後のデータを、ドライバ用表示データ２１０３として出力している（図１８参照）。

【０００６】分周回路２１２１は、同期信号２４０２に含まれているドットクロックを分周することで、表示データが有効な期間中、表示データ取り込みクロック２１１１を生成し、これを出力している（図１８参照）。

【０００７】また、遅延回路２１２２は、同期信号２４０２に含まれている水平同期信号を遅延させ、表示データラッチクロック２１０４と、イネーブル信号２１０５と、を生成し、出力している（図１８参照）。

【０００８】これらの信号のうち、ドライバ用表示データ２１０３、表示データ取り込みクロック２１１１は、カラム回路２１００へ出力されている。一方、イネーブル信号２１０５は走査駆動回路２１３１へ出力している。表示データラッチクロック２１０４は、カラム回路２１００と、走査駆動回路２１３１との両方に出力されている。

【０００９】カラム回路２１００は、表示データ取り込みクロック２１１１の立ち下がりにおいて、ドライバ用表示データ２１０３を取り込むものである。ここで、カラム回路２１００として使用している株式会社日立製作所製のカラム回路ＨＤ６６３１０は、出力を１６０本有するものであるため、該液晶表示装置では、ＨＤ６６３１０を１２個（＝１９２０／１６０）使用している。以下、カラム回路２１００－１～２１００－１２を総称して、カラム回路群２１３０と呼ぶ。カラム回路２１００は、イネーブル信号入力ＥＩＯ１がローレベルの時だけ、ドライバ用表示データ２１０３を取り込むようになっている。

【００１０】また、該カラム回路２１００は、６０画素分の表示データを取り込むと、イネーブル信号出力ＥＩＯ２がハイレベルからローレベルに変化するようになっている。そして、各カラム回路２１００のイネーブル信号入力ＥＩＯ１には、左隣に位置するカラム回路２１００のイネーブル出力信号ＥＩＯ２が入力されている。なお、最左端に位置するカラム回路２１００－１についてはイネーブル信号入力ＥＩＯ１を接地されている。な

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お、カラム回路ＨＤ６６３１０の内部構成については、後ほど具体的に説明する。

【００１１】カラム回路２１００－１が、１６０画素分の表示データ２１０３を取り込みを完了すると、そのイネーブル出力信号ＥＩＯ２はハイレベルからローレベルに変化する。すると、次段（右隣）のカラム回路２１００－２がイネーブルになる。そして、今度は当該カラム回路２１００－２が表示データ２１０３の取り込みを開始する。

【００１２】以後同様にして、左側に位置するカラム回路２１００から順次１６０画素ずつ表示データを取り込んで行く。

【００１３】そして、１ライン分のドライバ用表示データ２１０３を取り込み終わると、カラムカイロ群２１３０は、当該１ライン分の表示データに対応する表示電圧を液晶パネル２１３２に印加する。

【００１４】一方、走査駆動回路２１３１は、イネーブル信号２１０５に同期して、垂直ラインを順次走査している。

【００１５】すると、カラム回路２１００が出力する表示データ（後述するラッチ回路２３０３がラッチしているデータ）は、その時、走査駆動回路２１３１によって選択されているラインにおいて表示されることとなる。

【００１６】なお、ライン毎に表示データが変化しない場合でも、データの書き込みが行われている。

【００１７】次に、カラム回路ＨＤ６６３１０の概要を図１９を用いて説明する。

【００１８】カラム回路ＨＤ６６３１０には、４画素分の該入力表示データ２１０３がパラレルで入力される構成となっている。入力表示データ２１０３は、各画素について諧調データ３ビットである。また、液晶駆動電圧を出力するための信号線２１０１を１６０本備えている。

【００１９】ラッチアドレスカウンタ２３０１は、表示データ取り込みクロック２１１１の立ち下がりをカウントして、ラッチ信号を生成する。なお、表示データ取り込みクロック２１１１は、イネーブル信号入力ＥＩＯ１でマスクできるようになっている。イネーブル信号入力ＥＩＯ１がハイレベルの時には、ラッチ信号を生成しない。また、表示データ取り込みクロック２１１１を４０回カウントした後は、イネーブル信号出力ＥＩＯ２をローレベルにする。なお、後述するとおり、一度に４画素分の表示データを取り込むことができるため、４０回のカウントは、１６０（＝４×４０）画素分の表示データの取り込みに相当する。

【００２０】ラッチ回路２３０２は、４画素毎４０段に分割されている。該ラッチ回路２３０２は、ラッチアドレスカウンタ２３０１からのラッチ信号に同期して、ドライバ用表示データ２１００３を同時に４画素分だけ取り込む。

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【００２１】ラッチ回路２３０３は、１６０画素分のラッチ回路で構成されている。ラッチ回路２３０３は、ラッチ回路２３０２の取り込んだ表示データを、表示データラッチクロック２１０４に同期してラッチする。そして、このラッチしたデータを、１ライン時間保持する。

【００２２】レベルシフタ回路２３０４は、ラッチ回路２３０３がラッチした表示データをデコードし、液晶印加電圧を選択するためのセレクト信号を生成する。

【００２３】液晶駆動回路２３０５は、８種類存在する液晶駆動電圧２３０６のうちの１つをセレクト信号に従って選択し、該選択した電圧を印加電圧２１０１として液晶パネルのＸ電極へ出力する。

【００２４】以上述べたように、液晶表示装置における表示動作は、その大部分がカラム回路２１００への表示データのラッチ動作の繰り返しである。

【００２５】液晶表示装置の駆動方式には、この他にも、液晶パネルの水平方向を２つの領域に分け、各々の領域毎の表示データを同時に転送するというものがある。該駆動方式においては、表示メモリを２つ備え、一方に表示データを書き込んでいる時には、他方の表示メモリから表示データを読み込んで、該読み込んだ表示データをパラレルに出力している。このような技術については、例えば、特開平１－１１３７９３号公報、特開平２－１２６２８５号公報、特開平５－２３２８９８号公報に記載されている。

【００２６】

【発明が解決しようとする課題】現在では、液晶パネルにも高精細表示が求められるようになっている。これに対応するには、画素ピッチの微細化だけでなく、カラム回路の出力ピッチも微細化しなければならない。これは、カラム回路の上述したカスケード接続ができないからである。また、カラム回路自体の小面積化、また、カラム回路の出力を液晶パネル接続するＴＡＢの小ピッチ化等も図らなければならない。

【００２７】ところが、ＴＡＢと液晶パネルを微細化すると、その接合部分の位置合わせや接合技術に高度な技術を要することになり、生産コストが高くなるという別の問題を生じていた。そのため、従来の液晶駆動回路を用いつつ、高精細表示の液晶パネルに対応する技術が求められていた。

【００２８】本発明は、従来の液晶駆動回路を用いつつ、画素ピッチを微細化した液晶パネルに対応可能な表示コントローラを提供することを目的とする。

【００２９】

【課題を解決するための手段】本発明は上記目的を達成するためになされたもので、その第１の態様としては、Ｍ個のＹ電極と、Ｎ個のＸ電極とを備えた、アクティブマトリックス型の液晶パネルと、選択電圧と、非選択電圧と、複数種類の階調電圧とを生成する機能を備え、上記選択電圧を出力する選択電圧端子と、上記非選択電圧

を出力する非選択電圧端子と、上記階調電圧を出力する階調電圧端子とを備えた電源回路と、ｎ個（ｎ＜Ｎ）の出力端子を備え、上記電源回路から出力される上記階調電圧のうちのいずれかを、別途与えられたデータ列に対応して該出力端子毎に選択し、該選択した階調電圧を当該出力端子から出力するカラム回路と、上記Ｙ電極のいずれか一つに上記選択電圧を、また、その他のＹ電極には上記非選択電圧を印加するコモン手段と、構成要素がｎ個以下である複数のグループに上記Ｘ電極を分類し、該グループのうちいずれか一つを選択して、該選択されたグループに属するＸ電極のみを上記カラム回路の上記出力端子と予め定められた対応関係をもって接続するＸ電極スイッチ手段と、少なくとも、表示データと水平同期信号とが外部から入力されており、該外部から入力された表示データの順番を並べ替えて、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、上記カラム回路へ出力する表示コントローラと、を有することを特徴とする液晶表示装置が提供される。

【００３０】上記表示コントローラは、少なくとも１ライン分のデータを記憶可能な第１のメモリと、少なくとも１ライン分のデータを記憶可能な第２のメモリと、外部から入力されてくる表示データを取り入れ、上記第１のメモリまたは第２のメモリに書き込む書き込み手段と、上記第１のメモリと第２のメモリとのうち、その時点で上記書き込み手段による書き込み動作の実行対象となっていない方から、当該メモリに既に格納されている表示データを、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、読み出して出力する読み出し手段と、上記カラム回路が、あるグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力を開始する前に、上記Ｘ電極スイッチ手段による上記グループの選択を、該次のグループのＸ電極とカラム回路の出力端子とが接続されるように変更させる選択指示手段と、上記書き込み手段による上記表示データの書き込み動作の対象とされるメモリを、上記水平同期信号が有効になるのを契機として、上記第１のメモリと上記第２のメモリとの間で交互に切り替えさせる制御手段と、を含んで構成されてもよい。

【００３１】上記表示データの外部からの入力はパラレルで行われるものであり、上記外部から入力されてくる表示データを予め定められた画素数分だけ受け付けて、該受け付けた表示データを、当該表示データが対応するＸ電極の属するグループに基づいて分類して、該分類毎に出力する変換手段をさらに備え、上記書き込み手段は上記変換手段が出力する表示データを、上記第１のメモリまたは上記第２のメモリに書き込むものであってもよい。

【００３２】上記書き込み手段は、別途生成される書き込みクロックに同期して、上記書き込み動作を行うものであり、上記読み出し手段は、上記書き込みクロックとは非同期の別途生成される読み出しクロックに同期して、上記読み出しを行うものであり、上記制御手段は、上記書き込み手段による上記表示データの書き込み対象とされるメモリの切り替えを、上記水平同期信号に代わって、１画面分の表示データを書き込んだことを確認して行わせるものであり、上記第１のメモリおよび上記第２のメモリは、上記液晶パネル１画面分の表示データを記憶可能な記憶容量を備えてもよい。

【００３３】上記コモン手段は、ｍ個（ｍ＜Ｍ）の出力端子を備え、該出力端子のうちの１つを順次選択し、該選択された出力端子からは上記選択電圧を、他の出力端子からは非選択電圧を出力するコモン回路と、上記Ｙ電極を構成要素がｍ個以下である複数のグループに分け、いずれかのグループに属するＹ電極のみを選択的に上記コモン回路の上記出力端子と予め定められた対応関係をもって接続するとともに、その時点で上記コモン回路と接続されていないＹ電極を上記電源回路の非選択電圧端子に接続するＹ電極スイッチ手段とを備え、上記表示コントローラは、上記コモン回路がすべての出力端子を選択し終わる度ごとに、上記Ｙ電極スイッチ手段による上記グループの選択を変更させるものであること好ましい。

【００３４】上記第１のメモリおよび上記第２のメモリは、その記憶容量を変更可能に構成されていることがより好ましい。

【００３５】本発明の第２の態様としては、Ｍ個のＹ電極と、Ｎ個のＸ電極とを備えた、アクティブマトリックス型の液晶パネルと、ｎ個（ｎ＜Ｎ）の出力端子を備え、該出力端子から別途別途与えられたデータ列に対応した階調電圧を出力するカラム回路と、構成要素がｎ個以下である複数のグループに上記Ｘ電極を分類し、該グループのうちいずれか一つを選択して、該選択されたグループに属するＸ電極のみを上記カラム回路の上記出力端子と予め定められた対応関係をもって接続するＸ電極スイッチ手段と、を含んで構成された液晶表示装置の駆動に使用される表示コントローラにおいて、少なくとも１ライン分のデータを記憶可能な第１のメモリと、少なくとも１ライン分のデータを記憶可能な第２のメモリと、外部から入力されてくる表示データを取り入れ、上記第１のメモリまたは第２のメモリに書き込む書き込み手段と、上記第１のメモリと第２のメモリとのうち、その時点で上記書き込み手段による書き込み動作の実行対象となっていない方から、当該メモリに既に格納されている表示データを、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、読み出して出力する読み出し手段と、上記カラム回路が、あるグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力

を開始する前に、上記Ｘ電極スイッチ手段による上記グループの選択を、該次のグループのＸ電極とカラム回路の出力端子とが接続されるように変更させる選択指示手段と、上記書き込み手段による上記表示データの書き込み動作の対象とされるメモリを、上記水平同期信号が有効になるのを契機として、上記第１のメモリと上記第２のメモリとの間で交互に切り替えさせる制御手段と、を含んで構成されることを特徴とする表示コントローラが提供される。

【００３６】

【作用】電源回路は、選択電圧端子からは選択電圧を、非選択電圧端子からは非選択電圧を、階調電圧端子からは階調電圧端子を出力している。

【００３７】Ｘ電極スイッチ手段は、構成要素がｎ個以下である複数のグループに上記Ｘ電極を分類し、該グループのうちいずれか一つを選択して、該選択されたグループに属するＸ電極のみを上記カラム回路の上記出力端子と予め定められた対応関係をもって接続している。

【００３８】表示コントローラは、外部から入力された表示データの順番を並べ替えて、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、上記カラム回路へ出力する。表示コントローラは、例えば、以下のように構成することができる。

【００３９】書き込み手段は、外部から入力されてくる表示データを取り入れ、上記第１のメモリまたは第２のメモリに書き込んでいる。読み出し手段は、第１のメモリと第２のメモリとのうち、その時点で上記書き込み手段による書き込み動作の実行対象となっていない方から、当該メモリに既に格納されている表示データを、対応するＸ電極の属する上記グループが互いに一致する表示データの集まり毎に、順次、読み出して出力している。この時、制御手段は、書き込み手段による表示データの書き込み動作の対象とされるメモリを、水平同期信号が有効になるのを契機として、上記第１のメモリと上記第２のメモリとの間で交互に切り替えさせている。これにより、第１のメモリと第２のメモリとには、交互に、表示データが１ライン分ずつ書き込み／読み出しが行われて行く。並べ替えは、この書き込みあるいは読み出しの際に、各グループに対応したアドレスを指定して行くことで行う。

【００４０】カラム回路は、階調電圧のうちのいずれかを、表示コントローラから与えられるデータ列に対応して出力端子毎に選択し、該選択した階調電圧を当該出力端子から出力する。この時、表示コントローラの選択指示手段は、カラム回路が、あるグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力を開始する前に、Ｘ電極スイッチ手段によるグループの選択を、該次のグループのＸ電極とカラム回路の出力端子とが接続されるように変更させている。その結果、その時カラム回路の出力している階調電圧は、この時選択されているグループに属するＸ電極に印加されることになる。

【００４１】なお、表示データの外部からの入力はパラレルである場合には、表示データを、変換手段によって、グループ毎に分類し、該分類ごとに出力させるようにする。そして、書き込み手段は変換手段が出力する表示データを、上記第１のメモリまたは上記第２のメモリに書き込むようにすればよい。また、書き込み手段が同期するクロックと、読み出し手段が同期するクロックとが、互いに非同期出ある場合には、制御手段は、上記書き込み手段による上記表示データの書き込み対象とされるメモリの切り替えを、１画面分の表示データを書き込んだことを確認して行うようにする。そして、第１のメモリおよび上記第２のメモリは、上記液晶パネル１画面分の表示データを記憶可能な記憶容量を備えるようにする。

【００４２】一方、コモン手段は、Ｙ電極のいずれか一つに選択電圧を、また、その他のＹ電極には上記非選択電圧を印加する。該コモン手段は、例えば、以下のように構成できる。コモン回路は、該出力端子のうちの１つを順次選択し、該選択された出力端子からは上記選択電圧を、他の出力端子からは非選択電圧を出力している。Ｙ電極スイッチ手段は、Ｙ電極を構成要素がｍ個以下である複数のグループに分け、いずれかのグループに属するＹ電極のみを選択的に上記コモン回路の上記出力端子と予め定められた対応関係をもって接続する。また、その時点で上記コモン回路と接続されていないＹ電極を上記電源回路の非選択電圧端子に接続する。そして、表示コントローラは、コモン回路がすべての出力端子を選択し終わる度ごとに、上記Ｙ電極スイッチ手段による選択状況を変更させる。

【００４３】

【実施例】本発明の実施例を図面を用いて説明する。

【００４４】本発明の第１の実施例を図１から図６を用いて説明する。

【００４５】本実施例の液晶表示装置は、図１に示すとおり、液晶パネル１０１と、液晶パネル１０１のＸ電極を駆動するためのカラム回路１１０と、液晶パネル１０１のＹ電極を駆動するためのコモン回路１１２と、外部から入力されてくる各種信号および表示データ等に従って、カラム回路１１１０及びコモン回路１１２を作動させる表示コントローラ１０２と、電源回路１０９と、から構成されている。当然、これらは、各種信号等を授受するための信号線１０３，１０４，１０５，１０６，１０８，１２７，１２２～１２５、およびバス１１１，１１３，１１５，１２６，１１７，１０７によって接続されている。さらに、本実施例では、液晶パネル１０１とカラム回路１１０との接続を、表示コントローラ１０２からの指示に従って作動するスイッチ群１１８～１２１を介して行っている。本実施例は、このスイッチ群１１

８～１２１を設けたこと、及び、これに対応した表示制御を最大の特徴とするものである。

【００４６】なお、以下の説明においては説明文と図面との対応関係を判り易くするため、これら信号線やバスを通じて授受される信号を、当該信号線、バスの番号を付して呼ぶ場合がある。例えば、バス１０７を通じて入力される表示データを、表示データ１０７と呼ぶこととする。他の実施例の説明についても同様である。

【００４７】液晶パネル１０１は、３２０本のＸ電極と、２４０本のＹ電極とでマトリックスを構成し、その交点にスイッチング素子を持つアクティブマトリックス型のものである。

【００４８】表示コントローラ１０２は、外部から入力される表示データ１０７および各種制御信号に基づいて、液晶パネル１０１に表示を行うための表示データ１２６及び各種信号を生成するものである。外部から入力される制御信号には、垂直同期信号１０３と、水平同期信号１０４と、表示データの有効範囲を示すブランク信号１０５と、ドットクロック１０６とがある。表示データ１０７は、ドットクロック１０６に同期して、画面上における表示位置に従った順番で、シリアルで送られてくるものである。

【００４９】表示コントローラ１０２は、これら制御信号１０３～１０６、表示データ１０７に基づいて、交流化信号１０８、カラム制御信号１１５、コモン制御信号１１７、表示データ１２６、およびスイッチ群１１８～１２１を制御するスイッチ制御信号１２２～１２５を生成し出力している。

【００５０】本実施例の表示コントローラ１０２は、該表示データ１０７をスイッチ群１１８～１２１等の接続関係に対応して並べ替え、表示データ１２６として出力する機能を備えている。本実施例では、スイッチ群が４つあることに対応して、表示データを並べ替えた上で、４つのグループに分けて出力している。このグループ分けは、画面上における表示位置を、４の剰余系に従って分類することで行っている。これは、各スイッチ群１１８～１２１と、Ｘ電極との接続関係が、４の剰余系に従っていることに対応したものである。各グループ内では、表示位置が左側にあるものほど先に出力される。該表示コントローラ１０２及び該並べ替えの詳細については後ほど説明する。

【００５１】電源回路１０９は、液晶パネルへ印加する各種電圧（対向電極電圧１２７、階調電圧１１１、選択／非選択電圧１１３）を生成するためのものである。階調電圧１１１は、交流化信号１０８に同期して生成されて、カラム回路１１０に供給されている。該階調電圧１１１には、対向電極電圧１２７に対して、正極性のものと、負極性のものとがある。選択／非選択電圧１１３は、コモン回路１１２へ出力されている。

【００５２】カラム回路１１０は、バス１１１を通じて入力された階調電圧のうちいずれかを画素毎に選択し、該選択されたものを出力バス１１４（出力端子ｓ０～ｓ８０）から出力するものである。該階調電圧は、上述のスイッチ１１８群１１８～１２１によって、その時、出力バス１１４と導通状態とされている所定のＸ電極にのみ供給される。該カラム回路１１０は、表示コントローラ１０２の出力するカラム回路制御信号１１５によってその動作状態を制御されている。

【００５３】コモン回路１１２は、バス１１３を通じて入力される選択電圧／非選択電圧を、出力バス１１６を通じて液晶パネル１０１のＹ電極へ出力するものである。該コモン回路１１２は、表示コントローラ１０２の出力するコモン回路制御信号１１７によってその動作状態を制御されている。

【００５４】スイッチ群１１８～１２１は、カラム回路１１０の出力バス１１４を構成する出力端子ｓ０～ｓ８０と、液晶パネル１０１のＸ電極（電極ｘ０～ｘ３１９）との接続関係を、適宜変更するためのものである。各スイッチ群１１８～１２１は、それぞれ８０個のスイッチで構成されている。液晶パネル１０１の電極ｘ０～ｘ３１９は、左側からの位置を予め定められた規則（本実施例では、４の剰余系）に従って分類することで４つのグループに分けられている。スイッチ群１１８～１２１は、制御信号１２２～１２５からの指示に従ってＯＮ／ＯＦＦ状態をそれぞれ変更することで、適宜、いずれかの群に属するＸ電極のみをカラム回路の出力バス１１４と接続するようになっている。ここでは第１スイッチ群１１８に属するスイッチを、左側から順に、スイッチ１－１，スイッチ１－２、…、スイッチ１－８０と呼ぶ。第２スイッチ群に属するスイッチを、スイッチ２－１、スイッチ２－２、…、スイッチ２－８０と呼ぶ。第３スイッチ群１２０、第４スイッチ群１２１に属するスイッチについても同様の呼び方をする出力端子ｓ０～ｓ８０と、スイッチ群１８１～１２１と、電極ｘ０～ｘ３１９と、の具体適接続関係は以下のとおりである。出力端子ｓ０は、スイッチ１－１によって電極ｘ０と、スイッチ２－１によって電極ｘ１と、スイッチ３－１によって電極ｘ２と、スイッチ４－１によって電極ｘ３と、接続可能になっている。同様に、出力端子ｓ１は、スイッチ１－２，２－２，３－２，４－２によって、電極ｘ４，ｘ５，ｘ６，ｘ７と接続可能となっている。出力端子ｓ２～ｓ８０、電極ｘ８～ｘ３１９の間も、同様の関係を持って接続されている。

【００５５】従って、第１スイッチ群１１８（スイッチ１－１～１－８０）のみをＯＮに、他のスイッチ群１１９，１２０，１２１をＯＦＦにすることで、出力端子ｓ０～ｓ８０から出力される階調電圧を、電極ｘ０，ｘ４，ｘ８，ｘ１２，…，ｘ３１６へ印加できる。第２スイッチ群１１９（スイッチ２－１～２－８０）のみを、ＯＮにすれば、同様に出力端子ｓ０～ｓ８０から出力さ

れる階調電圧を、電極ｘ１，ｘ５，ｘ９，ｘ１１３，…，ｘ３１７へ印加できる。第３スイッチ群１２０（スイッチ３－１～３－８０）、第４スイッチ群１２１（スイッチ４－４～３－８０）についても、同様である。

【００５６】第１スイッチ群１１８の状態（ＯＮ／ＯＦＦ）は、表示コントローラ１０２の出力する第１制御信号１２２によって変更される。第２スイッチ群１１９の状態（ＯＮ／ＯＦＦ）は、第２制御信号１２３によって変更される。第３スイッチ群１２０の状態（ＯＮ／ＯＦＦ）は、第３制御信号１２４によって変更される。第４スイッチ群１２１の状態（ＯＮ／ＯＦＦ）は、第４制御信号１２５によって変更される構成となっている。

【００５７】次に、表示コントローラ１０２について、図２を用いてさらに詳細に説明する。　表示コントローラ１０２は、クロック制御部２０１、メモリ系制御バス２０２、メモリ制御部２０３、メモリ制御バス２０４、メモリ制御バス２０５、バス制御線２０６、メモリ２０７、メモリ２０８、データバス２０９，２１０、バスセレクタ２１１、ラッチ回路２１３を含んで構成されている。

【００５８】クロック制御部２０１は、垂直同期信号１０３、水平同期信号１０４、ブランク信号１０５、ドットクロック１０６に基づいて、交流化信号１０８、カラム制御信号１１５、コモン制御信号１１７、スイッチ制御信号１２２～１２５を生成するものである。さらに、クロック制御部２０１は、表示コントローラ１０２内を制御するメモリ系制御信号２０２、ラッチクロック２１４も生成している。

【００５９】メモリ系制御信号２０２は、読み出しクロックを含んで構成されている。ラッチクロック２１４は、カラム制御バス１１５の中のデータ転送クロックに同期したものである。また、後述の図４，図６における、データ転送クロック、出力クロックは、カラム制御信号１１５に含まれているものである。また、図６におけるＦＬＭ、ライン信号は、コモン制御信号１１７に含まれているものである。

【００６０】メモリ制御部２０３は、メモリ２０７，２０８へのデータの書き込み／読み出し、及び、バスセレクタ２１１の状態を制御するためのものである。そのため、メモリ制御部２０３は、メモリ系制御信号２０２に同期したメモリ制御信号２０４，２０５を生成し、各メモリ２０７，２０８へ出力している。メモリ制御信号２０４，２０５には、図３における、メモリ２０７，２０８を書き込み可能状態とするライトイネーブル信号と、読み出し可能状態とするリードイネーブル信号、データを書き込みアドレスを指定するアドレス信号、とが含まれている。

【００６１】さらに、メモリ制御部２０３は、バス制御信号２０６をバスセレクタ２１１へ出力している。メモリ制御部２０３は、メモリ２０７への書き込みを行う時には、バス制御信号２０６を”ハイ”に、一方、メモリ２０８に書き込みを行う時には、バス制御信号２０６を”ロー”にする。

【００６２】メモリ２０７およびメモリ２０８は、それぞれ１ライン分の表示データを記憶可能な記憶容量を有している。該メモリ２０７、２０８へのデータの書き込み、読み出しはデータバス２０９、データバス２１０を通じてなされる。

【００６３】上述の表示データの並べ替えは、該メモリ２０７（あるいは、２０８）への表示データの格納、読み出しに伴って行われる構成となっている。

【００６４】バスセレクタ２１１は、メモリ２０７，２０８のいずれか一方を選択して、表示データ１０７を書き込むためのものである。また、メモリ２０７またはメモリ２０８のいずれか一方を選択して、当該選択されたメモリに格納されている表示データを読み出して表示データ２１２としてラッチ回路２１３へ出力するものである。

【００６５】バス制御信号２０６が”ハイ”の時、バスセレクタ２１１は、表示データバス１０７とデータバス２０９とを、また、出力バス２１２とデータバス２１０とを接続状態にする。一方、バス制御信号２０６が”ロー”の場合、表示データバス１０７とデータバス２１０とを、また、出力バス２１２とデータバス２０９とを接続する。

【００６６】ラッチ回路２１３は、ラッチクロック２１４に従って、表示データ２１２を一時記憶するものである。ラッチ回路２１３は、この後、該記憶したデータを表示データ信号１２６としてカラム回路１１０へ出力する構成となっている。

【００６７】特許請求の範囲において言う”選択電圧端子”、”非選択電圧端子”、”階調電圧端子”とは、本実施例においては、電源回路１０９が選択電圧、非選択電圧、階調電圧を出力する端子及び、これに接続されている信号線、バスに相当するものである。”Ｘ電極スイッチ手段”とは、スイッチ群１１８～１２１に相当するものである。また、Ｘ電極を分けたグループとは、いずれのスイッチ群に接続されているかによって規定されるものである。

【００６８】”第１のメモリ”および”第２のメモリ”とは、本実施例ではメモリ２０７とメモリ２０８とに相当するものである。”書き込み手段”、”読み出し手段”とは、クロック制御部２０１、メモリ制御部２０２、バスセレクタ２１１およびこれらをつなぐバス等が密接に連携して動作することで実現されるものである。”選択指示手段”とは、クロック２０１に相当するものである、”制御手段”とは、メモリ制御部２０２、クロック制御部２０１、バスセレクタ２１１が連携して動作することで実現されるものである。

【００６９】本実施例の液晶表示装置の動作を説明す

る。

【００７０】まず、表示コントローラ１０２およびカラム回路１１０の動作を、図２乃至図５を用いて説明する。ここでは、外部から入力されて来た表示データ１０７をメモリ２０７に書き込みつつ、これと並行して、メモリ２０８に格納されている表示データを読み出す場合について説明する。

【００７１】ブランク信号１０５が、"有効"を意味するローレベルになる。すると、メモリ制御回路２０３は、バス制御信号２０６を"ハイ"にする。また、これと同時に、メモリ制御部２０３は、メモリ制御信号２０４中のライトイネーブル信号を"有効"にするとともに、当該データを格納するアドレスを指定する。

【００７２】すると、バス制御信号２０６が"ハイ"となったことで、バスセレクタ２１１は、表示データ１０７を、メモリ２０７へ出力する。これを受けて、メモリ２０７は、当該表示データを、メモリ制御信号２０４において指定されているアドレスに格納する。

【００７３】この場合、書き込もうとするデータが最初のデータ（０番目のデータ）であれば、メモリ制御回路２０３はアドレス"０"を指定する。次のデータ（１番目のデータ）に対しては、アドレス８０を指定する。さらに、この次に入力されてくる２番目のデータに対してはアドレス１６０を、３番目のデータに対しては、アドレス２４０を指定する。４番目のデータは、アドレス１を指定する。５番目のデータに対してはアドレス８１を、６番目のデータに対してはアドレス１６１を、７番目のデータに対してはアドレス２４１を指定する。つまり、各グループのスタートアドレスを８０以上ずらした上で、各グループ内においては、アドレスを１ずつ１インクリメントしてゆくようにする。

【００７４】アドレス指定をこのように行うことで、図５に示すとおり、アドレス０からアドレス７９までの領域には、第１スイッチ群１１８を通じてＸ電極に出力されるデータが格納されることになる。また、アドレス８０から１５９までの領域には、第２スイッチ群１１９を通じて出力されるデータが格納されることになる。同様に、アドレス１６０～２３９には、第３スイッチ群１２０に対応するデータが、また、アドレス２４０～３１９には、第４スイッチ群１２１に対応するデータが格納される。

【００７５】以上述べたメモリ２０７への表示データの書き込み動作と並行して、メモリ２０８に格納されているデータのラッチ回路２１３への出力も行われている。

【００７６】図３において、水平同期信号１０４が"有効"になると、クロック制御部２０１は、メモリ制御信号２０２中の読み出しクロック（図示せず）を８０個づつ出力する。

【００７７】また、メモリ制御部２０３は、データを読み出してくるアドレスを、該読み出しクロックに同期してメモリ制御信号２０５中において指定する。この場合のアドレスの指定は、アドレス０から１ずつ順次インクリメントしてゆくものとする。

【００７８】すると、最初に、第１スイッチ群１１８に対応する表示データが、メモリ２０８からバスセレクタ２１１を通じてラッチ回路２１３へ出力されてくる。続いて、第２スイッチ群１１９、第３スイッチ群１２０、第４スイッチ群１２１に対応するデータが順次出力されてくる。

【００７９】ラッチ回路２１３は、出力されてきたデータをラッチクロック２１４に同期して記憶する。ラッチ回路２１３は、次のラッチクロック２１４が有効になるまで、ラッチしたデータを表示データバス１２６に出力し続ける。

【００８０】読み出しクロックを８０個出力した後、クロック制御部２０１は、カラム制御信号１１５に含まれている、出力クロックを"有効"にする。なお、この出力クロックは、階調電圧を出力するタイミングをカラム回路１１０へ指示するためのものである。また、これと並行して、クロック制御部２０１は、スイッチ制御信号１２２～１２５によって、その時、表示データ１２６として出力しているデータの対応するスイッチ群をＯＮに、また、他のスイッチ群はＯＦＦにする。例えば、その時の表示データ１２６が、第１スイッチ群１１８に対応したもの（図５においては、アドレス８０～１５９）であれば、第１スイッチ群１１８をＯＮに、第２、第３、第４スイッチ群１１９，１２０，１２１をＯＦＦにする。これにより、カラム回路１１０は、その時の表示データ信号１２６に対応した階調電圧を、次の出力クロックが有効になるまでの期間、所定のＸ電極にのみ出力することになる。なお、スイッチ制御信号１２２～１２５の出力のタイミングは、カラム回路１１０が、前の表示データに対応する階調電圧を出力し終わってから、次のる表示データの階調電圧の出力を開始するまでであれば、特に限定されない。場合によっては、目的とする表示データの階調電圧の出力を開始した後であっても、構わない。適宜、実際の各部回路の特性等にあわせて設定すれば良い。

【００８１】第１スイッチ群１１８を通じて階調電圧がＸ電極（電極ｘ０，ｘ４，ｘ８，…，ｘ３１６）に印加されている間は、第２スイッチ群１１９に対応するデータ（図５においては、アドレス８０～１５９）がメモリ２０８から読み出されている。この後も、同様に、第２スイッチ群１１９を通じて階調電圧が出力されている間は、第３スイッチ群１２０に対応するデータ（図５においては、アドレス１６０～２３９）の読み出しが、さらに、該第３スイッチ群１２０を通じて階調電圧が出力されている間は、第４スイッチ群１２１に対応するデータ（図５においては、アドレス２４０～３１９）の読み出しが行われる。第４制御信号１２５は、コモン回路１１

２が次のＹ電極を選択する前に無効にされる。このようにして、表示データ１０７のメモリ２０７への書き込み、およびメモリ２０８からの表示データ１２６の出力が、１ライン分だけ終わる。

【００８２】この後、次の水平同期信号１０４が有効になると、今度は、表示データ１０７はメモリ２０８へ書き込まれる。そして、メモリ２０７から次の行の表示データが読み出される。このようにメモリ２０７，２０８の間で交互に読み出し／書き込み動作を繰り返すことにより、表示コントローラ１０２からは、表示データ１０７から１水平期間遅れて表示データ１２６が出力されている。

【００８３】以上の動作を繰り返すことで、表示データに対応した諧調電圧が、順次、液晶パネル１０１に出力される。

【００８４】次に、コモン回路１１２の動作について、図１と図６を用いて説明する。

【００８５】図６のように、コモン制御信号１１７のうち、最初のラインを示すファーストラインマーカ（以下、＂ＦＬＭ＂と略す）および選択ラインの切り替えを指示するライン信号が有効になると、コモン回路１１２は、出力バス１１６を通じて電極ｙ０に選択電圧を出力する。一方、他のＹ電極（ここでは、電極ｙ１～ｙ２３９）には、非選択電圧を出力する。すると、電極ｙ０のスイッチング素子だけが導通状態になる。その結果、その時Ｘ電極に印加されている階調電圧は、電極ｙ０に対応する行の画素にだけ印加される。

【００８６】ライン信号が次回有効になると、コモン回路１１２は今度は電極ｙ１に選択電圧を出力する。電極ｙ０および電極ｙ１～ｙ２３９には非選択電圧を出力する。これにより、その時Ｘ電極に印加されている階調電圧は、電極ｙ１に対応する行の画素にだけ印加される。この動作を電極ｙ２３９まで繰り返すことで、１画面分の表示が完了する。この後、表示コントローラ１０２は、ＦＬＭを有効にして、再び電極ｙ０から順次選択電圧を出力してゆく。

【００８７】以上、述べてきた動作を繰り返すことにより、本実施例の液晶表示装置は、表示データに対応した表示を行うことが可能になる。

【００８８】本発明の第２の実施例を図７から図１０を用いて説明する。

【００８９】本実施例は、表示コントローラへの表示データの入力、及び表示コントローラからの表示データの出力が、パラレルで行なわれる点が実施例１とは異なるものである。なお、以下の説明は実施例１との相違点を中心に行い、同じ機能部分については説明を省略する場合がある。

【００９０】先ず概要を説明する。

【００９１】本実施例の液晶表示装置は、図７に示すとおり、液晶パネル７０１と、液晶パネル７０１のＸ電極を駆動するためのカラム回路７０４と、液晶パネル７０１のＹ電極を駆動するためのコモン回路１１２と、外部から入力されてくる表示データなどに従ってカラム回路７０４およびコモン回路１１２を作動させる表示コントローラ７０２と、電源回路１０９と、から構成されている。また、カラム回路７０４と液晶パネル７０１のＸ電極との間には、実施例１におけるスイッチ群１１８～１２１と同様の構成をもって、スイッチ群７０７～７１０が設けられている。当然、これらおよび後述の各部は、各種信号等を授受するための信号線、バスによって接続されている。

【００９２】液晶パネル７０１は、９６０画素×２４０ラインのアクティブマトリックス型のものである。

【００９３】表示コントローラ７０２には、垂直同期信号１０３、水平同期信号１０４、ブランク信号１０５、ドットクロック１０６、表示データ７０３が入力されている。表示コントローラ７０２は、これらの入力に基づいて、交流化信号１０８、カラム制御信号１１５、コモン制御信号１１７、表示データ７０５、およびスイッチ群７０７～７１０を制御するスイッチ制御信号１２２～１２５を生成し出力している。

【００９４】本実施例における表示データ７０３は、ドットクロック１０６に同期して、３画素分が同時に（パラレルで）転送されてくるものである。表示コントローラ７０２は、この表示データ７０３を各スイッチ群７０７～７１０に対応した順番に並べ換え、これを表示データ７０５としてカラム回路１１０へ出力している。表示データ７０５も、３画素分が同時にパラレルに送られている。表示データバス７０３，７０５は当然、これに対応したものとなっている。

【００９５】カラム回路７０４は、表示データ７０５を記憶し、該記憶した表示データに対応した階調電圧を、カラム制御信号バス１１５中の出力クロックに同期して、出力バス７０６から出力することで、液晶パネル７０１への表示を行わせるものである。本実施例のカラム回路７０４は、３画素分がまとめて送られてくる表示データ７０５を１度に記憶可能となっている。カラム回路７０４は、２４０個の出力を備えているため、該カラム回路７０４は、この記憶動作を８０回繰り返すことで、２４０出力分の表示データを記憶している。

【００９６】コモン回路１１２、電源回路１０９については、実施例１と同様であるため説明を省略する。

【００９７】次に、表示コントローラ７０２について図８を用いてさらに詳細に説明する。

【００９８】表示コントローラ７０２は、図８に示すとおり、クロック制御部２０１、メモリ制御部８０１、ラッチクロックバス８０２、データラッチ回路８０３、バス８０４、メモリ制御信号バス８０５，８０６、それぞれが１ライン分の表示データを記憶できるメモリ８０７、８０８、メモリ８０７，８０８のデータバス８０

９，８１０、バスセレクタ８１１、バスセレクタ８１２の出力バス８１２、データラッチ回路８１３、バス制御信号線２０６を含んで構成されている。

【００９９】メモリ制御部８０１は、クロック制御部２０１から供給されるメモリ系制御信号２０２に基づいて、ラッチクロック８０２、メモリ制御信号８０５、８０６を生成している。そして、ラッチクロック８０２はデータラッチ回路８０３へ、また、メモリ制御信号８０５，８０６はメモリ８０７，８０８へ出力している。ラッチクロック８０２は、データラッチ回路８０３による表示データ７０５の取り込みのタイミングを規定するものであり、ドットクロック１０６に同期した信号が含まれている。メモリ制御信号８０５、８０６は、それぞれメモリ８０７，８０８の動作状態（読み出し／書き込み）を指定・変更するための信号と、読み出し／書き込みのタイミングを規定するためのクロックと、読み出し／書き込みを行うアドレスと、を含んで構成されている。

【０１００】データラッチ回路８０３は、３画素分づつパラレルで入力されてくる表示データ７０３を、スイッチ群７０７～７１０に対応して並び換えるためのものである。該データラッチ回路８０３は、並び変えた後の表示データを出力バス８０４から出力している。データラッチ回路８０３については、この後図９を用いてさらに詳細に説明する。特許請求の範囲において言う"変換手段"とは、本実施例では該データラッチ回路８０３に相当するものである。

【０１０１】メモリ８０７，８０８は、それぞれ１ライン分の表示データを格納可能なものである。該メモリ８０７，８０８は、メモリ制御部８０１から入力されるメモリ制御信号８０５，８０６によってその動作状態（書き込み／読みだし）が変更されるようになっている。また、表示データの入出力は、データバス８０９，８１０を通じて行われる。

【０１０２】メモリ８０７，８０８への表示データ８０４の格納は、メモリ制御信号８０５，８０６中のクロックに同期して行われる。また、メモリ８０７，８０８からの表示データの読み出しは、メモリ制御信号８０５，８０６の読み出しクロックに同期して行われる構成となっている。

【０１０３】バスセレクタ８１１は、出力バス８０４と、出力バス８１２と、データバス８０９と、データバス８１０と、の接続関係をバス制御信号２０６に従って変更するためのものである。つまり、表示データ８０４をメモリ８０７へ格納すると同時に、メモリ８０８から表示データの読み出しを行う場合には、出力バス８０４とデータバス８０９とを、また、出力バス８１２とデータバス８１０とを接続する。逆に、表示データ８０４をメモリ８０８へ格納すると同時に、メモリ８０７からは表示データの読み出しを行う場合には、出力バス８０４とデータバス８１０とを、また、出力バス８１１２とデータバス８０９とを接続する。

【０１０４】ラッチ回路８１３は、出力バス８１２を通じてメモリ８０７（あるいは８０８）から読みだされた表示データをラッチし、表示データ７０５として出力するものである。ラッチは、ラッチクロック２１４に従って行なわれている。表示データ７０５の出力は、カラム回路制御信号１１５に含まれているデータ転送クロックに同期して行なわれている。

【０１０５】データラッチ回路８０３を図９を用いてさらに詳細に説明する。

【０１０６】データラッチ回路８０３は、ラッチ回路９０１～９０４、ラッチ回路９１０～９１３、出力バス９０５～９０８、出力バス９１４～９１７、データセレクタ９１８から構成されている。

【０１０７】ラッチ回路９０１～９０４およびラッチ回路９１０～９１３は、３画素分の表示データを１度にラッチ可能なものである。これらは、ラッチしたデータをそれぞれの出力バス９０５～９０８、出力バス９１４～９１７から出力可能となっている。

【０１０８】データセレクタ回路９１８は、出力バス９１４～９１７を通じて出力されてくる表示データの中から所定のものを選択し、これを表示データ８０４として、ラッチクロック８０２に同期して出力するものである。該選択は、表示データ８０４が、スイッチ群７０７～７１０に対応したものとなるような順番で行われる。該選択の順番は、実際にはメモリ制御部８０１の出力してくるラッチクロック８０２によって指定されている。該指定の詳細は動作説明において行う。

【０１０９】本実施例の動作を、図７～図１０を用いて説明する。ここでの説明は、表示コントローラ７０２を中心として行う。

【０１１０】図８において、表示コントローラ７０２にドットクロック１０６に同期して表示データ７０３が送られてくる。すると、データラッチ回路８０３は、ラッチクロックバス８０２に従って、表示データ７０３を４回、つまり１２（３×４）画素分の表示データをラッチする。更に、データラッチ回路８０３は、ラッチした１２画素分の表示データを、スイッチ群７０７～７１０に対応した順番に並べ換えて、表示データ８０４として出力する。

【０１１１】該表示データ８０４は、ある１つのスイッチ群に属する表示データが３画素分づつまとめられている。つまり、最初に、第１スイッチ群７０７に対応したデータだけが３画素分出力される。続いて、第２スイッチ群７０８に対応するデータだけが３画素分出力される。この後も、同様に、第３スイッチ群、第４スイッチ群に対応するデータだけが、それぞれ３画素分づつ出力される。なお、データラッチ回路８０３の動作については、図９、図１０を用いてこの後、さらに詳細に説明す

る。

【０１１２】該表示データ８０４は、メモリ８０７とメモリ８０８とのうちいずれかへ格納される。バス制御信号２０６が”ロー”になっていれば、バスセレクタ８１１は、出力バス８０４と出力バス８０９を導通状態にしている。そのため、この時データラッチ回路８０３から出力される表示データ８０４は、メモリ８０７へ書き込まれる。バス制御信号２０６が”ハイ”になっている場合には、この時出力される表示データ８０４はメモリ８０８へ書き込まれる。

【０１１３】データを書き込むアドレスは、各スイッチ群７０７～７１０に対応して、メモリ制御部８０１が指定する。例えば、最初の３画素分のデータは、第１スイッチ群７０７に対応するものであるため、アドレス０を指定する。続く、３画素分のデータは第２スイッチ群７０８に対応するものであるため、アドレス８０を指定する。続く、第３スイッチ群７０９に対応するデータにはアドレス１６０を、第４スイッチ群７１０に対応するデータには、アドレス２４０を指定する。本実施例の液晶パネルはＸ電極を９６０本備えているため、各スイッチ群に割り当てるアドレスの初期値は８０以上間隔をあける必要がある。

【０１１４】なお、図１０において、メモリ制御部８０１は、ブランク信号１０５が有効になってからドットクロック１０６の５クロック目の立ち下がりに同期して、メモリ制御信号８０５のライトイネーブル信号を有効にする。そして、以後は、ドットクロック１０６に同期して、ライトイネーブル信号の状態（有効（ロー）／無効（ハイ）を制御している。図１０では、表示データ８０４がメモリ８０７へ書き込まれ、メモリ８０８に対しては以下において述べる読み出し動作が行われている場合の様子を示した。

【０１１５】以上の格納動作と並行して、メモリ８０８からの表示データの読み出しおよびカラム回路７０４への転送が行なわれている。

【０１１６】読み出すデータのアドレスは、メモリ制御部８０１から入力されているメモリ制御信号８０６により指定されている。水平同期信号１０４が有効になると、メモリ制御部８０１は、メモリ系制御信号２０２中の読み出しクロックに同期して、該指定するアドレスを０から７９まで順次インクリメントしてゆく。該読み出しクロックは、８０クロック出力後にマスクされる。読み出されたデータは、出力バス８１０、バスセレクタ８１１、出力バス８１２を通じて、データラッチ回路８１３へ出力される。

【０１１７】データラッチ回路８１３は、該表示データ８１２を、ラッチクロック２１４に従ってラッチする。この後、これをカラム回路制御信号１１５中のデータ転送クロックに同期して、表示データ７０５としてカラム回路７０４へ出力する。

【０１１８】カラム回路７０４は、表示データ７０５を順次記憶してゆく。そして、カラム制御信号バス１１５の出力クロックが有効になると、出力バス７０６に階調電圧を出力する。

【０１１９】出力クロックが有効になった後は、読み出しクロックが再び８０クロック分”有効”となる。この時には、メモリ制御部８０１は、アドレス”８０”から”１５９”までの表示データをメモリ８０８から読み出させる。この後も、同様の処理を繰り返してゆく。

【０１２０】以上の読み出し動作を繰り返すことにより、メモリ８０８に格納されていた１ライン分の表示データに対応した階調電圧を出力できる。

【０１２１】次に、データラッチ回路８０３の動作を、図９、図１０を用いてさらに詳細に説明する。

【０１２２】ここでは、液晶パネル７０１上において表示される位置を明確にするため、表示データには、ｎ－ｍという番号を付することにする。ｎは、９６０本のＸ電極（電極ｘ０～電極ｘ９５９）を左側から順に４本毎に区切った場合に、当該表示データの出力される電極の属する領域が左側から何番目の領域であるかを示す番号である。ｍは、当該表示データの出力される電極がその領域内で左側から何番目に位置するかを示す番号である。但し、ｎ，ｍは、０から始まるものとする。ある表示データｎ－ｍが出力される電極のＸ電極全体の中での位置は３ｎ＋ｍで表せる。言い替えれば表示データｎ－ｍは、電極ｘ(3n+m)に出力されるデータである。例えば、表示データ０－０は、液晶パネル７０１の電極ｘ０の表示データである。表示データ０－１は電極ｘ１、表示データ０－２は電極ｘ２に出力されるべきものである。

【０１２３】データラッチ回路８０３の各部は、ラッチクロック８０２に従ってその動作タイミングが決定されている。該ラッチクロック８０２には、５種類のラッチクロック（以下、それぞれを”第１ラッチクロック”～”第５ラッチクロック”という）が含まれている。

【０１２４】図１０に示すとおり、第１～第４ラッチクロックは、ドットクロック１０６の４サイクル毎に有効とされる。これらは第１クロックから順番に、ドットクロック１０６の１サイクル分ずつ位相が遅れている。第５ラッチクロックは、ドットクロック１０６の４サイクル毎に１回有効にされるものである。該第５ラッチクロックは、第４ラッチクロックよりも、ドットクロック１０６の半サイクル分だけ位相が遅れている。

【０１２５】図１０において、ブランク信号１０５が有効になると、ドットクロック１０６の最初の立ち下がりに同期して、第１ラッチクロックが有効になる。すると、ラッチ回路９０１は、これに同期して、表示データ７０３のうちの表示データ０－０～表示データ０－２をラッチする。これに続いて、ラッチ回路９０２～ラッチ回路９０４も同様に、第２ラッチクロック～第４ラッチ

クロックに同期して、表示データ１－０～３－２までの１２画素分の表示データをラッチする。

【０１２６】ラッチ回路９０１～９０４は、このラッチした表示データを、第５ラッチクロックに同期して１度にラッチ回路９１０～９１４に出力する。ラッチ回路９１０～９１４はこれをラッチし、第５ラッチクロックが次回" 有効" になるまで、出力バス９１４～９１７から出力しつづける。

【０１２７】データセレクタ９１８は、ラッチ回路９０１～９０４から同時に出力されて来ている１２画素分のデータのうち、第１スイッチ群７０７に対応した表示データ列（ここでは電極ｘ０，ｘ４，ｘ８対応した表示データ０－０，１－１，２－２）だけを選択し、これを表示データ８０４としてバスセレクタ８１１へ出力する。この場合の出力は、次回の第１ラッチクロックに同期して実行される。

【０１２８】続いて、データセレクタ９１８は、第２スイッチ群７０８に対応した表示データ列だけを選択し、これを表示データ８０４としてバスセレクタ８１１へ出力する。この場合の、出力は、第２ラッチクロックに同期して行われる。以下同様に、データセレクタ９１８は、第３ラッチクロックに同期して第３スイッチ群７０９に対応した表示データを、第４ラッチクロックに同期して第４スイッチ群７１０に対応した表示データを、表示データ８０４として出力する。

【０１２９】以上説明した第２の実施例によれば、パラレルで入力されてくる表示データに対しても、カラム回路７０４等を変更することなく、液晶パネルの高精細化へ対応できる。

【０１３０】本発明の第３の実施例を説明する。

【０１３１】該第３の実施例は、メモリからのデータ読み込みクロックと、メモリへのデータ書き込みクロックとが、互いに非同期である点が第２の実施例とは異なるものである。

【０１３２】本実施例の液晶表示装置は、図１１に示すとおり、液晶パネル７０１と、液晶パネル７０１のＸ電極を駆動するためのカラム回路７０４と、液晶パネル７０１のＹ電極を駆動するためのコモン回路１１２と、外部から入力されてくる表示データ等に従って、カラム回路７０４及びコモン回路１１２を作動させる表示コントローラ１１０１と、電源回路１０９と、スイッチ群７０７～７１０と、を含んで構成されている。さらに、本実施例では、表示コントローラ１１０１に外部クロック１１０３を供給する発振器１１０２を備えている。該外部クロック１１０３は、後述するとおり、メモリからの表示データの読み出しクロックの基にされるものである。

【０１３３】既に述べたとおり、表示コントローラ１１０１は、各種入力信号１０３，１０４，１０５，１０６、表示データ７０３に加え、発振器１１０２から入力される外部クロック１１０３が入力されている。表示コントローラ１１０２は、これらの入力に基づいて、表示データ７０５および各種信号１１５，１２２～１２５，１０８，１１７等を生成し、外部クロック１１０３に同期して出力している。

【０１３４】表示コントローラ１１０１の詳細を図１２を用いて説明する。

【０１３５】表示コントローラ１１０１は、図１２に示すとおり、クロック制御部１２０１、クロック制御部１２０３、メモリ制御部１２０５、バスセレクタ１２０８、メモリ１２１３，１２１４、データラッチ回路８０３、データラッチ回路８１３を含んで構成されている。また、これらの各部の間を接続し、データ、信号の授受を行うための各種バス、信号線を備えている。なお、図を簡単にするため、図１２においては、図１１における信号１１５，１２２～１２５，１０８，１１７をまとめて、信号１１２６として描いている。

【０１３６】クロック制御部１２０１は、垂直同期信号１０３、水平同期信号１０４、ブランク信号１０５、ドットクロック１０６に基づいて、書き込み制御信号１２０２、ラッチクロック８０２、を生成するものである。

【０１３７】書き込み制御信号１２０２には、垂直同期信号１０３、水平同期信号１０４、書き込みクロックが含まれている。垂直同期信号１０３および水平同期信号１０４は、表示データ８０４が、何ライン目のデータであるかをメモリ制御部１２０５が判断するために用いられる。書き込みクロックは、表示データ８０４が有効となっている時間範囲を、メモリ制御部１２０５に知らせるためのものである。

【０１３８】クロック制御部１２０３は、外部クロック１１０３に同期した、メモリ読み込み制御信号１２０４、信号１２１６、ラッチクロック２１４を生成するものである。

【０１３９】メモリ制御部１２０５は、メモリ１２１３，１２１４へのデータの書き込み、および、これらからのデータの読み出しを制御するものである。該メモリ制御部１２０５は、書き込み制御信号１２０２、読み込み制御信号１２０４に基づいて、ドットクロック１０６に同期したメモリ書き込み制御信号１２０６と、外部クロック１１０３に同期したメモリ読み込み制御信号１２０７と、バス制御信号２０６と、を生成しこれをセレクタ１２０８へ出力する構成となっている。

【０１４０】メモリ書き込み制御信号１２０６、メモリ読み込み制御信号１２０７は、それぞれリードイネーブル信号、ライトイネーブル信号、アドレス信号、データ信号とから構成されている（図１３参照）。読み出しイネーブル信号は、読み出し完了を示すためのものである。なお、バス制御信号２０６及びリードイネーブル信号は、バス１２０４を通じてクロック制御部１２０３にも出力されている。

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【０１４１】データラッチ回路８０３、データラッチ回路８１３は、実施例２と同様の機能を有するものである。

【０１４２】メモリ１２１３，１２１４は、ぞれぞれ１画面分の表示データを記憶可能な容量を備えたものである。メモリ１２１３，１２１４内での表示データの配置の仕方は、基本的には実施例１、２と同様である（図５参照）。但し、本実施例では、データを１画面分記憶するようになっているため、図１４に示すとおり、各ラインのデータを、液晶パネルの走査線の本数分（本実施例では、２４０本分）だけ並べて配置したものとなっている。このようなデータの配置は、メモリ制御部１２０５からのアドレスの指定の仕方によって実現される。

【０１４３】バスセレクタ１２０８は、バス制御信号２０６に従って、バス８０４と、バス１２１５と、バス１２１１とバス１２１２との接続関係を変更するものである。また、書き込み制御信号バス１２０６と、読み出し制御信号バス１２０７と、メモリ制御バス１２０９，１２１０との接続関係を変更するものである。

【０１４４】このバスセレクタ１２０８は、バス制御信号２０６が”ハイ”の時には、表示データ８０４はメモリ１２１３に書き込まれ、メモリ１２１４からは表示データの読み出しが行われるようにする。つまり、メモリ制御バス１２０９と書き込み制御信号バス１２０６とを、また、出力バス８８０４とデータバス１２１１とを、導通状態とする。さらに、出力バス１２１５とメモリデータバス１２１２とを、また、メモリ制御バス１２１０とメモリ書き込み信号バス１２０７とを、導通状態とする。

【０１４５】一方、バス制御信号２０６が”ロー”の時には、表示データ８０４はメモリ１２１４に書き込まれ、メモリ１２１３からは表示データの読み出しが行われるようにする。つまり、メモリ制御バス１２１０と書き込み制御信号バス１２０６とを、また、出力バス８０４とデータバス１２１２とを、導通状態とする。さらに、出力バス１２１５とメモリデータバス１２１１とを、また、メモリ制御バス１２０９とメモリ書き込み信号バス１２０７とを、導通状態とする。

【０１４６】本実施例の動作を図１３を用いて説明する。

【０１４７】図１１において、本実施例の動作は、交流化信号１０８、カラム制御信号バス１１５、コモン制御信号バス１１７、第１制御信号１２２、第２制御信号１２３、第３制御信号１２４、第４制御信号１２５、表示データ７０５が、外部クロック１１０３に同期して出力されること以外は、実施例２と同様である。従って、ここでは、表示コントローラ１１０１の内部動作についてのみ説明する。

【０１４８】クロック制御部１２０１，１２０３は、外部から入力されてくる信号１０３，１０４，１０５，１０６，１１０３に基づいて、各種信号８０２，１２０２，１１２０４，２１４，１２１６を出力している。

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【０１４９】また、メモリ制御部１２０５は、書き込み制御信号１２０２と読み込み制御信号１２０４から、メモリ書き込み制御信号１２０６、メモリ読み込み制御信号１２０７を生成し、セレクタ１２０８へ出力している。また、バス制御信号２０６をセレクタ１２０８へ出力している。

【０１５０】データラッチ回路８０３は、クロック制御部１２０１から入力されてくるラッチクロック８０２に同期して表示データ７０３を取り込み、これを並べ変えた上で、各スイッチ群７０７～７１０に対応した表示データ８０４として出力する。該並べ替えの詳細は、実施例２と同様である。ある１つのスイッチ群に対応する３画素分のデータが、スイッチ群ごとに順次、表示データ８０４として出力されている。

【０１５１】メモリ制御部１２０５は、セレクタ１２０８によって、１画面分の表示データ８０４を、メモリ１２１３とメモリ１２１４とのいずれかに格納させる。またこれと並行して、クロック制御部１２０３から出力されてくる読み出しクロックに同期しつつ、メモリ１２１３（あるいは１２１４）から１画面分の表示データを読み出させる。該表示データの読み出しは、他の実施例と同様、その時データの書き込み動作が行われていない方のメモリから行われる。

【０１５２】データラッチ回路８１３は、メモリ１２１３（あるいは１２１４）から読み出された表示データをラッチクロック２１４に同期してラッチする。そして、カラム制御信号１１５（図１２では信号１２１６）に含まれている転送クロックに同期して表示データを表示データ７０５として出力する。

【０１５３】図１３に示すとおり、メモリ制御部１２０５は、読み出しを完了すると、メモリ制御信号１２０７中のリードイネーブル信号を無効（本実施例では、”ロー”）にする。このリードイネーブル信号を受けたクロック制御部１２０３は、読み出しクロックの出力を休止する。

【０１５４】１画面分の表示データの、メモリ１２１３への格納およびメモリ１２１４からの読み出しが完了すると、図１３に示すとおり、メモリ制御部１２０５はバス制御信号２０６の状態（ハイ／ロー）を変更する。

【０１５５】すると、これに対応してセレクタ１２０８が作動し、表示データ８０４が格納されるメモリと、表示データが読み出されるメモリとが、次回は入れ替わることになる。また、クロック制御部１２０３は、バス制御信号２０６の状態変更に対応して自らを初期化する。そして、次画面の表示に備えて、再び、信号１２１６の生成を始める。さらに、クロック制御部１２０３は、読み出しクロックのメモリ制御部１２０５への出力を再開する。該読み出しクロックを受けたメモリ制御部１２０

５は、該読み出しクロックに同期して、アドレス" ０"から順次表示データを読み出す。

【０１５６】以上の動作を繰り返すことにより、本実施例の液晶表示装置は、非同期の２系統のクロックを持ちながらも、液晶パネル７０１への表示を可能としている。

【０１５７】第４の実施例を説明する。

【０１５８】該第４の実施例は、コモン回路と液晶パネルのＹ電極との間に、コモン回路の出力を選択するスイッチ群を配置し、これを表示コントローラによって制御する点が、実施例１とは異なっている。他の点については、基本的には実施例１と同様である。該実施例は、コモン回路の出力数が、液晶パネルのライン数より少ない場合に適用されるものである。

【０１５９】本実施例の液晶表示装置を図１５を用いて説明する。

【０１６０】液晶パネル１０１自体は、実施例１と同様のものである。但し、本実施例では、２４０本備えるＹ電極を２つのグループに分けて、その選択／非選択電圧の印加を制御されている。以下、図１５における上半分の領域に位置するＹ電極を第１コモンバス１６１０と、一方、下半分の領域に位置するＹ電極を第２コモンバス１６１１と呼ぶ。

【０１６１】スイッチ群１６０６～１６０９は、液晶パネルのＹ電極と、コモン回路１６０３の出力バス１６０４と、電源回路１０９からの非選択電圧信号線１６０５との接続関係を変更するためのものである。

【０１６２】電源回路１０９の生成する非選択電圧は、走査電圧バス１１３の途中から枝分かれして出ている非選択電圧信号線１６０５を通じても出力されている。該非選択電圧信号線１６０５は、上述の第２スイッチ群１６０７を通じて液晶パネル第１コモンバス１６１０と、また、第４スイッチ群１６０９を通じて第２コモンバス１６１１と接続可能に構成されている。

【０１６３】コモン回路１６０３は出力バス１６０４を構成する出力端子ｙ０～ｙ１１９のうち、いずれかに選択電圧を、他には非選択電圧を、出力するものである。いずれの出力端子から選択電圧を出力するかは、表示コントローラ１６０１から入力されるコモン制御信号１６０２によって指示されている。

【０１６４】本実施例のコモン回路１６０３の出力バス１６０４は、第１スイッチ群１６０６を通じて第１コモンバス１６１０と、第３スイッチ群１６０８を通じて第２コモンバス１６１１と接続可能になっている。

【０１６５】表示コントローラ１６０１は、コモン回路１６０３を制御するためのコモン制御信号１６０２を生成し出力している。さらに、スイッチ群１６０６～１６０９を制御するための第１制御信号１６１２、第２制御信号１６１３を出力する構成となっている。これらの制御信号１６１２，１６１３は、図２のクロック制御部２０１が生成している。表示コントローラ１６０１の内部構成は、基本的には図２と同様である。当然、スイッチ群１１８～１２１を制御するための第１制御信号１２２～第４制御信号１２５も出力している。

【０１６６】表示コントローラ１６０１は、第１コモンバス１６１０に属するＹ電極のうちのいずれかに選択電圧を印加する場合には、第１スイッチ群１６０６および第４スイッチ群１６０９をＯＮに、一方、第２スイッチ群１６０７及び第３スイッチ群１６０８をＯＦＦにするようになっている。これにより、第１コモンバス１６１０には、コモン回路１６０３からの出力が印加され、第２コモンバス１６１１には非選択電圧信号１６０５が印加される。逆に、第２コモンバス１６１１に属するＹ電極のいずれかに選択電圧を印加する場合には、第１スイッチ群１６０６及び第４スイッチ群１６０９をＯＦＦに、一方、第２スイッチ群１６０７および第３スイッチ群１６０８をＯＮにする。これにより、第１コモンバス１６１０には非選択電圧信号１６０５が印加され、第２コモンバス１６１１にはコモン回路１６０３からの出力が印加される。

【０１６７】特許請求の範囲において言う" Ｙ電極スイッチ手段"とは、スイッチ群１６０６～１６０９によって実現されるものである。Ｙ電極の" グループ"とは、第１コモンバス１６１０、第２コモンバス１６１１に相当するものである。

【０１６８】本実施例の動作を、図１５、図１６を用いて説明する。

【０１６９】本実施例の動作は、コモン回路１６０３の動作以外は基本的に上記第１の実施例と同じである。そのため、ここではコモン回路１６０３の動作のみを説明する。

【０１７０】第１コモンバス１６１０に属するＹ電極のうちのいずれかを選択すべき期間中、表示コントローラ１６０１は、第１制御信号１６１２を" 有効"（ハイ）に、また、第２制御信号１６１３を" 無効"（ロー）とする。その結果、第１スイッチ群１６０６および第４スイッチ群１６０９はＯＮ（導通状態）に、一方、第２スイッチ群１６０７および第３スイッチ群１６０８はＯＦＦ（遮断状態）になる。この状態では、第１コモンバス１６１０に属するＹ電極には、コモン回路１６０３の出力する選択／非選択電圧１６０４が、一方、第２コモンバス１６１１に属するＹ電極には、非選択電圧１６０５が印加されることとなる。コモン回路１６０３は、この間、選択電圧を出力する出力端子を、ライン信号に同期して順次、ｙ０→ｙ１→ｙ２→・・・→ｙ１９９と変更することで、第１コモンバス１６１０の範囲内で走査を行っている。

【０１７１】第１コモンバス１６１０に属するＹ電極（電極ｙ０～ｙ１１９）に対する走査が終わった後（つまり、電極ｙ１９９を選択した後）、表示コントローラ

１６０１は、今度は、第２制御信号１６１３を" 有効" （ハイ）に、また、第１制御信号１６１２を" 無効" （ロー）とする。その結果、第１スイッチ群１６０６および第４スイッチ群１６０９はＯＦＦ（遮断状態）に、一方、第２スイッチ群１６０７および第３スイッチ群１６０８はＯＮ（導通状態）になる。この状態では、第１コモンバス１６１０に属するＹ電極には、非選択電圧１６０５が、一方、第２コモンバス１６１１に属するＹ電極には、コモン回路１６０３の出力する選択／非選択電圧１６０４が印加されることとなる。その結果、コモン回路１６０３の出力する選択電圧が印加されるＹ電極は、ｙ１２０→ｙ１２１→ｙ１２２→・・・→ｙ２３９と、順次、変更されてゆくことになる。

【０１７２】なお、表示コントローラ１６０１は、第１制御信号１６１２および第２制御信号１６１３の有効（ハイ）／無効（ロー）変更を、ＦＬＭ，ライン信号のタイミングに基づいて行っている。図１６に示した例では、コモン回路１６０３は、コモン制御信号１６０２中のＦＬＭ信号がハイとなっている期間中に、ライン信号が有効になるのを契機として、出力端子ｙ０へ選択電圧を出力するようになっている。コモン回路１６０３が、次回、出力端子ｙ０へ選択電圧を出力するのは、ライン信号１６０２中のクロックが１２０クロック分出力された後、つまり、電極ｙ１２０へ選択電圧を印加するときである。

【０１７３】本実施例では、コモン回路１６０３の出力バスが液晶パネルのＹ電極数より少ない場合でも、液晶パネルの電極ｙ０から電極ｙ２３９まで順次走査することができる。

【０１７４】以上説明した第１～第４の実施例によれば、液晶パネルの高精細化へ容易に対応できる。また、液晶パネルの画素数やライン数を増加させる変更があった場合でも、その増加分に合わせて、メモリの記憶容量を増加させることで対応できる。

【０１７５】表示データの有効データ数が、液晶パネルの表示数より多い場合に、表示画像のうちの予め定められた領域部分のみを液晶パネルに表示させることも可能である。これを実現するには、液晶パネルに表示させる画像領域の範囲を示す座標値を記憶するレジスタを、表示コントローラに設ける。そして、入力された表示データの表示位置と、該レジスタに格納されている座標値とを比較し、レジスタ内において指定されている画像領域についての表示データのみをメモリに記憶すればよい。このようにすればアスペクト比が液晶パネルと異なっている画像も表示できる。

【０１７６】上記実施例では、表示データのメモリへの書き込み時に、並べ替えを行っていたが、逆に読み出し時に並べ替えを行うようにしても良い。例えば、書き込み時には、通常通り入力された順に表示データを並べて格納する。そして、読み出し時には、ある一つのスイッチ群に対応する一連の表示データを読みだす際には、アドレスを４ずつインクリメントしてゆけばよい。第１のスイッチ群に対応するデータを読みだす際には、アドレス０，４，８…を指定する。

【０１７７】本実施例では、表示コントローラを一つのＬＳＩにする事で、小型化できた。

【０１７８】

【発明の効果】本発明によれば、液晶駆動回路であるコモン回路、カラム回路の出力ピッチを小さくすることなく、液晶パネルの高精細化に対応できる。

【０１７９】書き込みクロックと、読み出しクロックが非同期のクロックの場合にも、１画面分のメモリを持つことで対応可能である。

【図面の簡単な説明】

【図１】本発明の第１の実施例である液晶表示装置の構成図である。

【図２】表示コントローラ１０２の内部構成を示すブロック図である。

【図３】メモリ２０７，２０８へのデータ書き込み／読み出しのタイミングチャートである。

【図４】スイッチ群１１８～１２１を作動させる制御信号１２２～１２５のタイミングチャートである。

【図５】メモリ２０７，２０８内での表示データの配置状態を示すマップである。

【図６】コモン回路１１２を制御する信号のタイミングチャートである。

【図７】本発明の第２の実施例である液晶表示装置の全体ブロック図である。

【図８】表示コントローラ７０２の内部構成を示すブロック図である。

【図９】データラッチ回路８０３の内部構成を示すブロック図である。

【図１０】メモリ２０７，２０８への表示データの格納／読み出し動作のタイミングチャートである。

【図１１】本発明の第３の実施例である液晶表示装置の全体ブロック図である。

【図１２】表示コントローラ１１０１の内部構成を示すブロック図である。

【図１３】メモリ１２１３，１２１４への表示データの格納／読み出し動作のタイミングチャートである。

【図１４】メモリ１２１，１２１４中における表示データの配置の様子を示すメモリマップである。

【図１５】本発明の第４の実施例である液晶表示装置の全体ブロック図である。

【図１６】コモン回路１６０３の出力電圧と、ｙ電極へ印加される電圧との関係を示すタイミングチャートである。

【図１７】従来例の液晶表示装置の構成図である。

【図１８】従来例のタイミングチャートである。

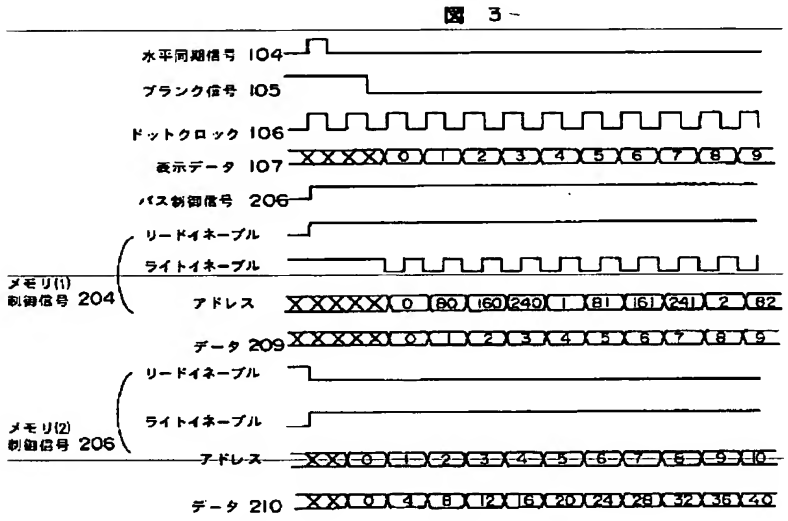
【図１９】従来例のカラム回路ＨＤ６６３１０の構成図

である。

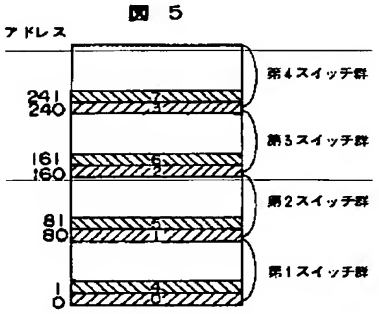
【符号の説明】

１０１…液晶パネル、１０２…表示コントローラ、１０３…垂直同期信号、１０４…水平同期信号１０５…ブランク信号、１０６…ドットクロック、１０７…表示データバス、１０８…交流化信号１０９…電源回路、１１０…カラム回路、１１１…諧調電圧バス、１１２…コモン回路、１１３…走査電圧バス、１１４…出力バス、１１５…カラム制御信号バス、１１６…出力バス、１１７…コモン制御バス１１８…第１スイッチ群、１１９…第２スイッチ群、１２０…第３スイッチ群、１２１…第４スイッチ群、１２２…第１制御信号、１２３…第２制御信号、１２４…第３制御信号、１２５…第４制御信号、１２６…表示データバス、１２７…対向電圧線、２０１…クロック制御部、２０２…メモリ系制御バス、２０３…メモリ制御部、２０４…メモリ制御バス、２０５…メモリ制御バス、２０６…バス制御信号、２０７…メモリ、２０８…メモリ、２０９…データバス、２１０…データバス、２１１…バスセレクタ、２１２…出力バス、２１３…ラッチ回路、２１４…ラッチクロック、７０１…液晶パネル、７０２…表示コントローラ、７０３…表示データバス、７０４…カラム回路、７０５…表示データバス、７０６…出力バス、７０７…第１スイッチ群、７０８…第２スイッチ群、７０９…第３スイッチ群、７１０…第４スイッチ群、８０１…メモリ制御部、８０２…ラッチクロックバス、８０３…データラッチ回路、８０４…出力バス、８０５…メモリ制御信号バス、８０６…メモリ制御信号バス、８０７…メモリ、８０８…メモリ、８０９…データバス、８１０…データバス、８１１…バスセレクタ、８１２…出力バス、８１３…データラッチ回路、９０１～９０４…ラッチ回路、９０５～９０８…出力バス、９１０～９１３…ラッチ回路、９１４～９１７…出力バス、９１８…データセレクタ回路、１１０１…表示コントローラ、１１０２…発振器、１１０３…外部クロック、１２０１…クロック制御部（１）、１２０２…書き込み制御信号バス、１２０３…クロック制御部（２）、１２０４…読み込み制御信号バス、１２０５…メモリ制御部、１２０６…メモリ書き込み信号バス、１２０７…メモリ読み込み制御信号バス、１２０８…バスセレクタ、１２０９…メモリ制御信号バス、１２１０…メモリ制御信号バス、１２１１…メモリデータバス、１２１２…メモリデータバス、１２１３…メモリ、１２１４…メモリ、１２１５…データバス、１２１６…制御信号バス、２１００…カラム回路、２１０１…信号線、２１０３…ラッチ回路、２１０４…クロック、２１０５…イネーブル信号、２１１０…ドライバ制御手段、２１１１…クロック、２１２０…データ変換回路、２１２１…分周回路、２１２２…遅延回路、２１３０…カラム回路群、２１３１…走査駆動回路、２１３２…液晶パネル、２４０１…表示データ、２４０２…同期信号、２３０１…ラッチアドレスカウンタ、２３０２…ラッチ回路、２３０３…ラッチ回路、２３０４…レベルシフタ回路、２３０５…液晶駆動回路、２３０６…液晶駆動電圧

【図３】

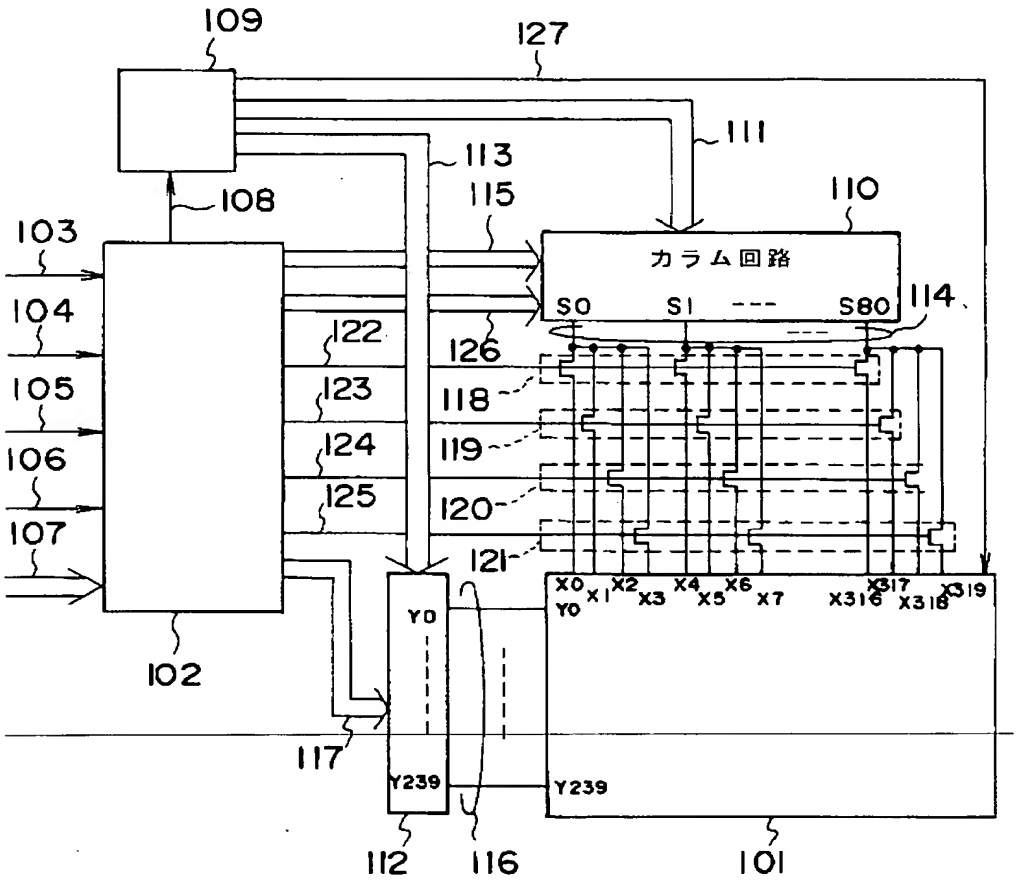


【図５】



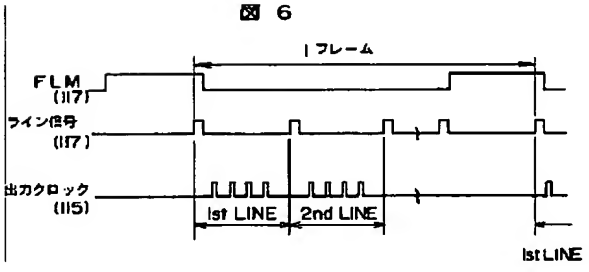
【図1】

図 1



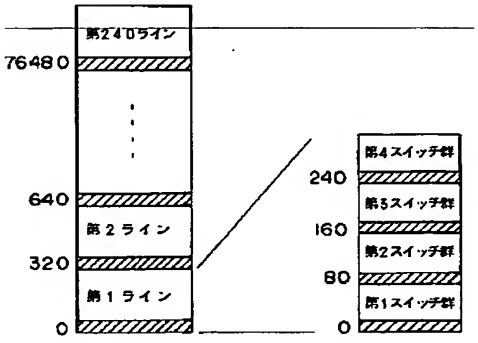
【図6】

図 6



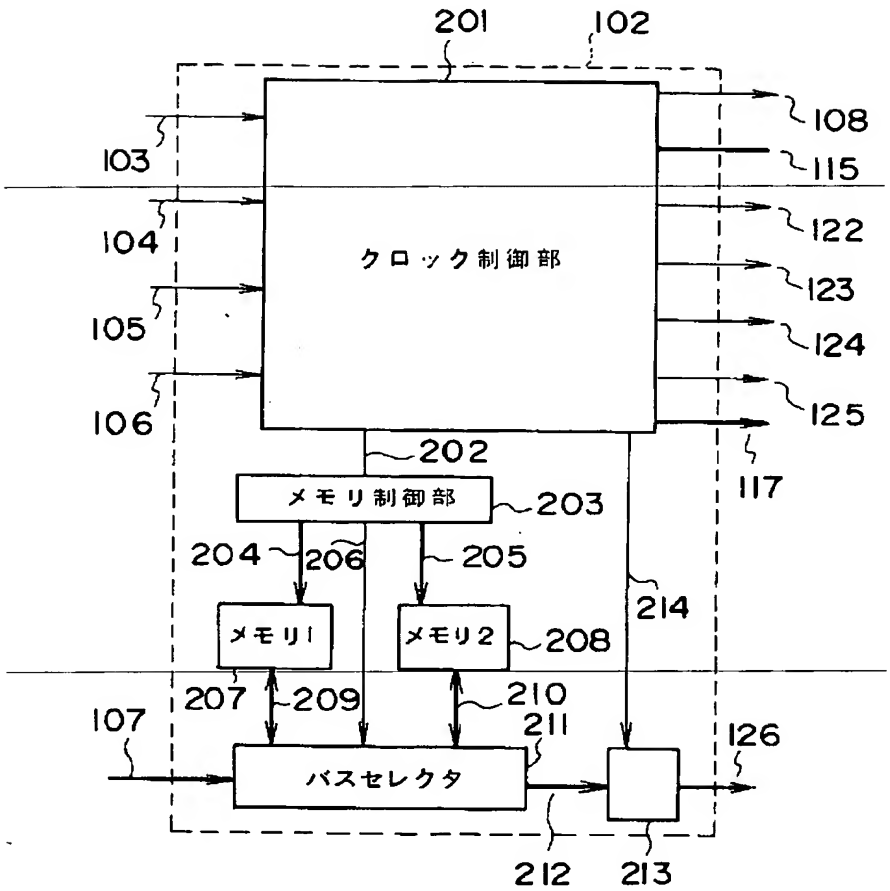
【図14】

図 14



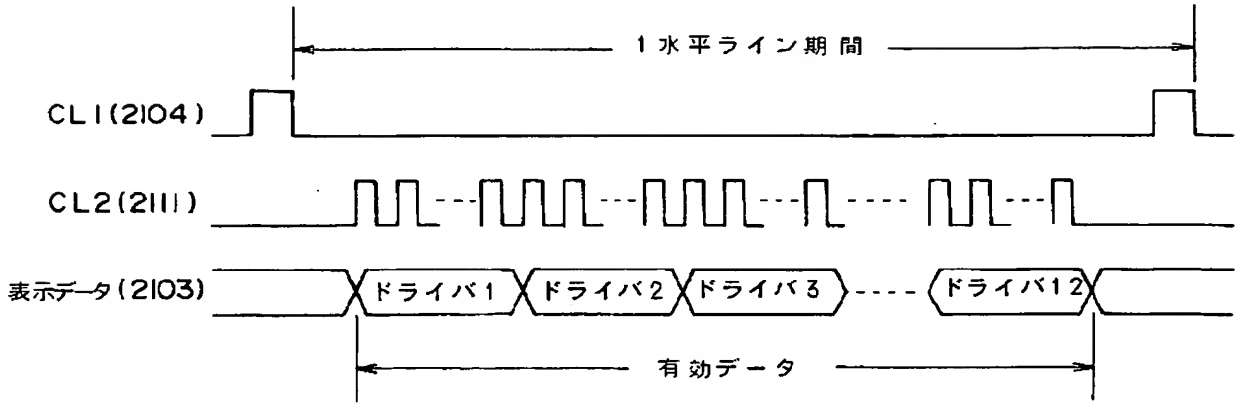
【図2】

図 2


201
102
108
103
115
104
クロック制御部
122
123
105
124
106
125
202
117
メモリ制御部
203
204
206
205
214
メモリ1
メモリ2
208
207
209
210
211
107
126
バスセレクタ
212
213

【図18】

図 18


1水平ライン期間
CL1(2104)
CL2(2111)
表示データ(2103)
ドライバ1
ドライバ2
ドライバ3
ドライバ12
有効データ

【図４】

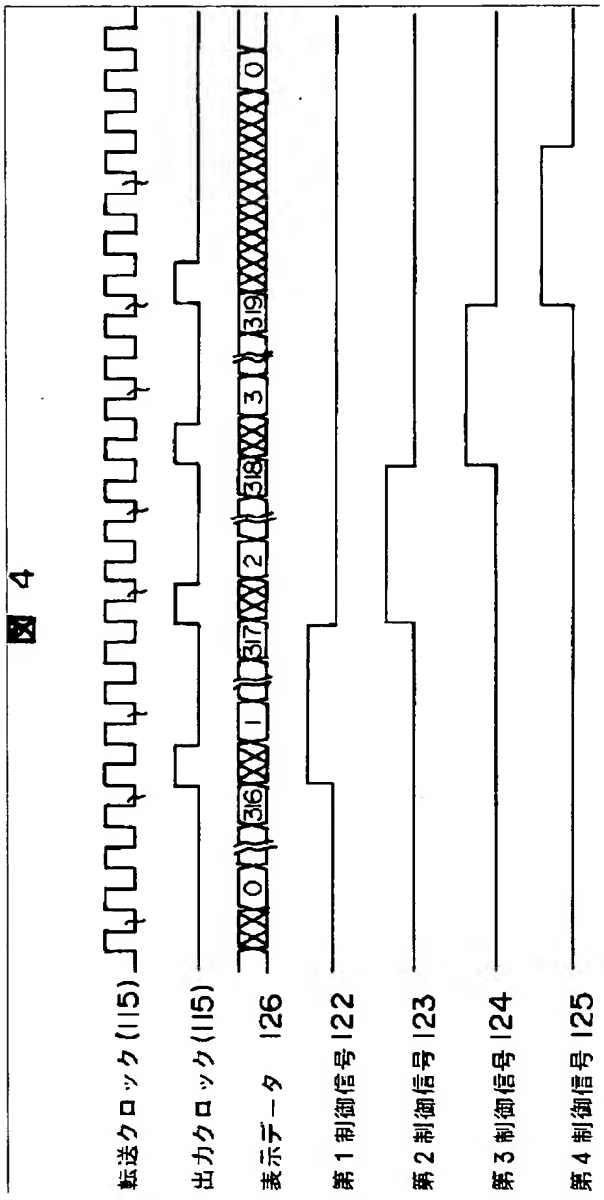
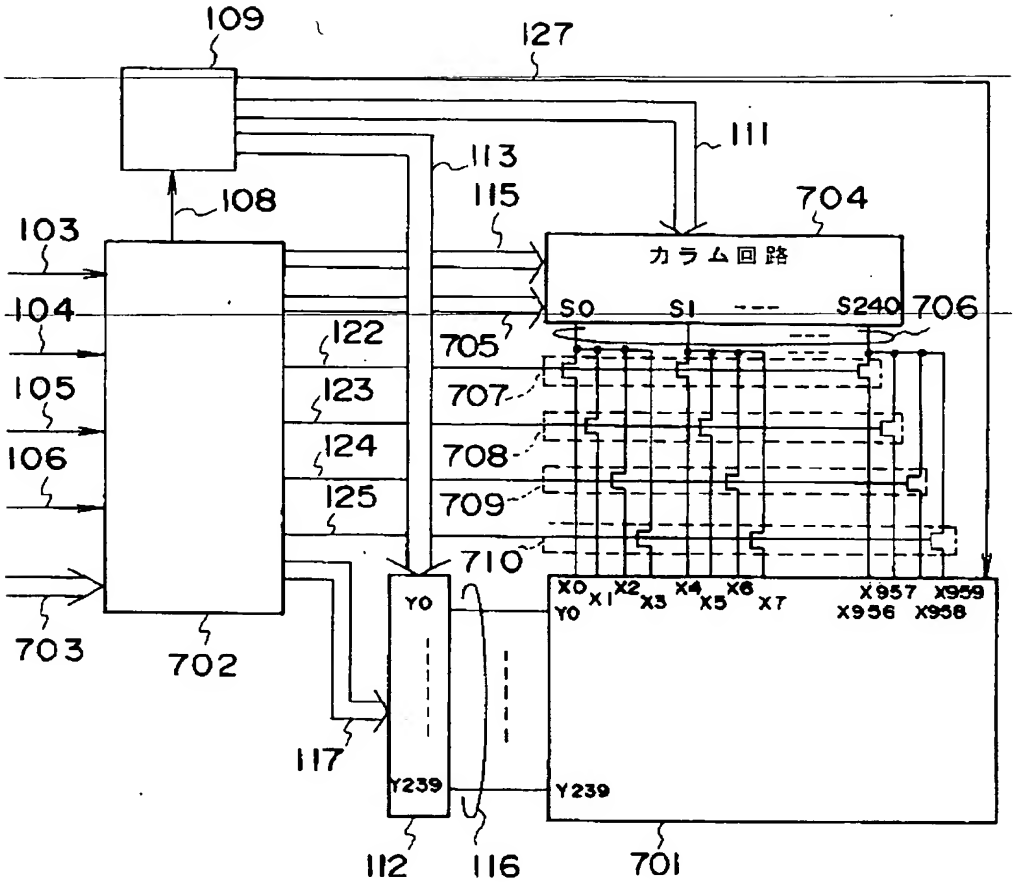


図 4
転送クロック(115)
出力クロック(115)
表示データ 126
第１制御信号122
第２制御信号123
第３制御信号124
第４制御信号125

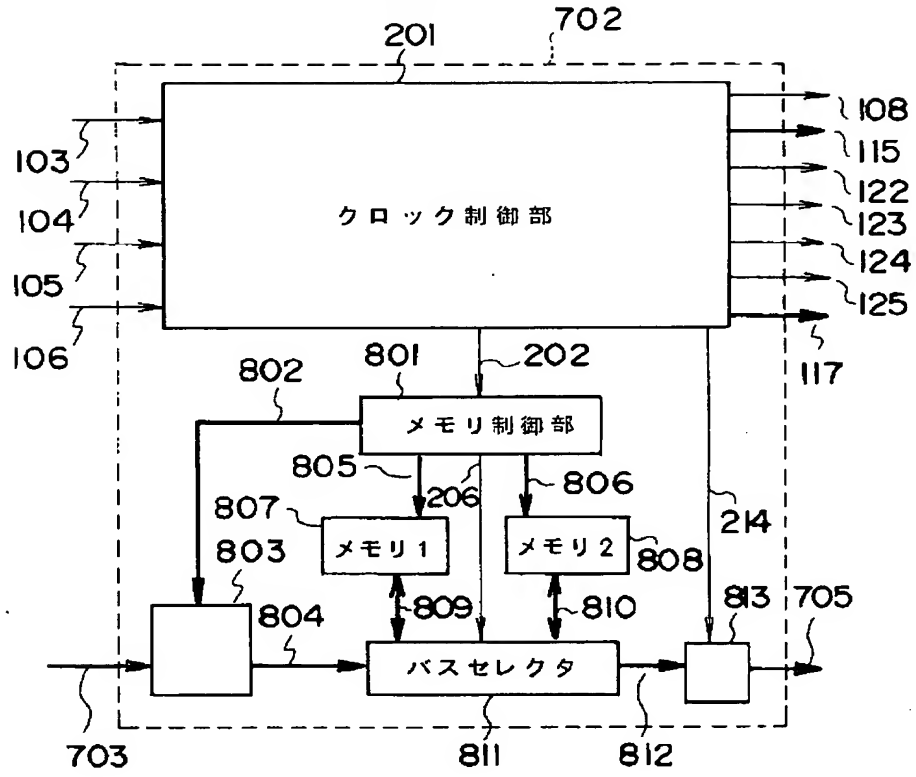
【図7】

図 7


109
127
111
113
115
108
704
103
カラム回路
104
S0
S1
S240
706
122
705
105
123
707
106
124
708
125
709
710
X0
X1
X2
X3
X4
X5
X6
X7
X957
X959
X956
X958
Y0
Y0
703
702
117
Y239
Y239
112
116
701

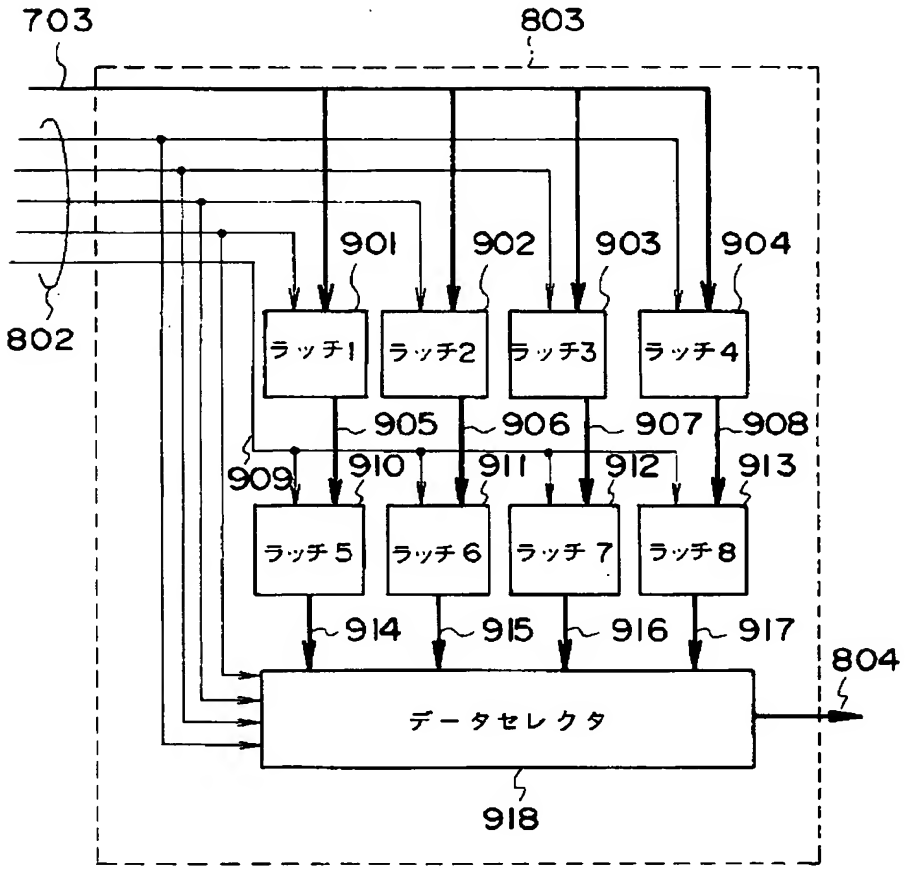
【図8】

図 8


201
702
103
104
105
106
クロック制御部
108
115
122
123
124
125
117
802
801
202
メモリ制御部
805
206
806
807
214
メモリ1
メモリ2
803
808
804
809
810
813
705
バスセレクタ
703
811
812

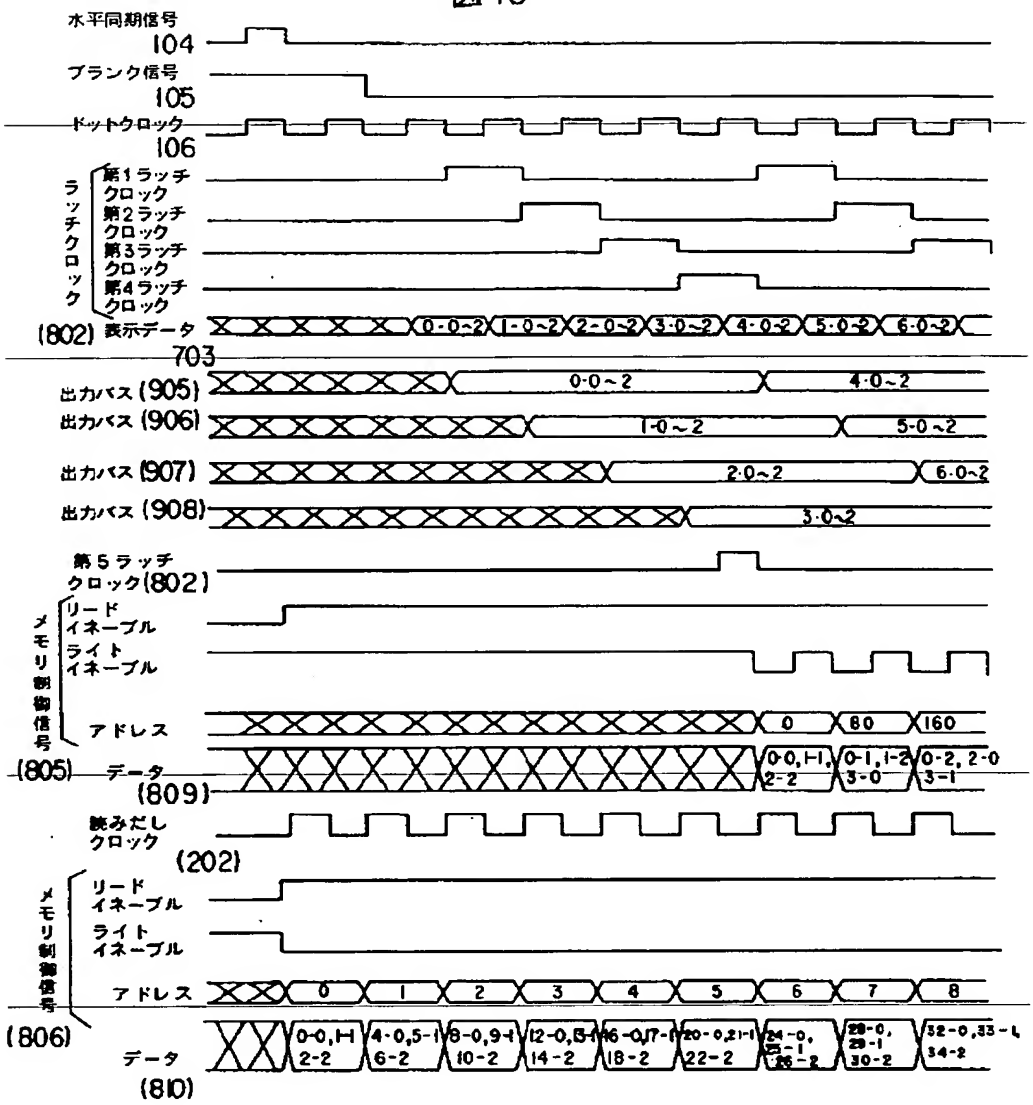
【図9】

図9


703
803
802
901
902
903
904
ラッチ1
ラッチ2
ラッチ3
ラッチ4
905
906
907
908
909
910
911
912
913
ラッチ5
ラッチ6
ラッチ7
ラッチ8
914
915
916
917
804
データセレクタ
918

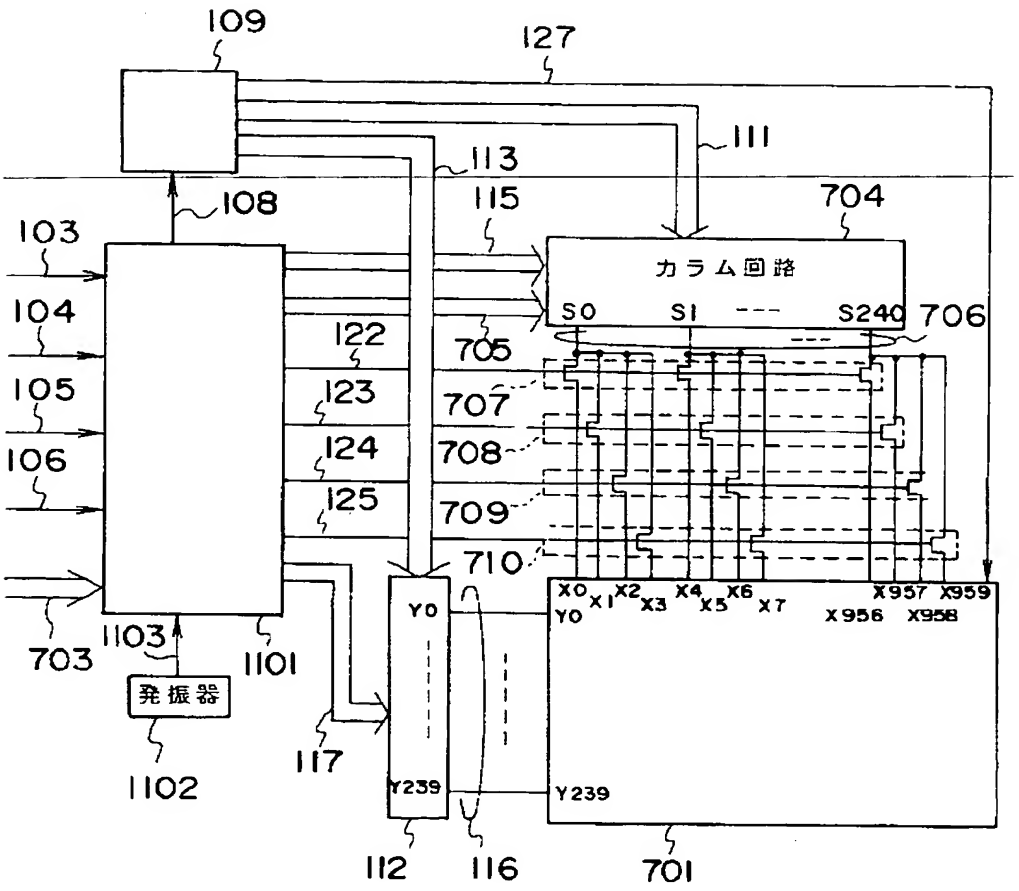
【図１０】

図 10


水平同期信号
104
ブランク信号
105
ドットクロック
106
ラッチクロック
第1ラッチクロック
第2ラッチクロック
第3ラッチクロック
第4ラッチクロック
(802)
表示データ
0-0~2
1-0~2
2-0~2
3-0~2
4-0~2
5-0~2
6-0~2
703
出力バス(905)
出力バス(906)
出力バス(907)
出力バス(908)
第5ラッチクロック(802)
メモリ制御信号
リードイネーブル
ライトイネーブル
アドレス
(805)
データ
(809)
読みだしクロック
(202)
(806)
(810)

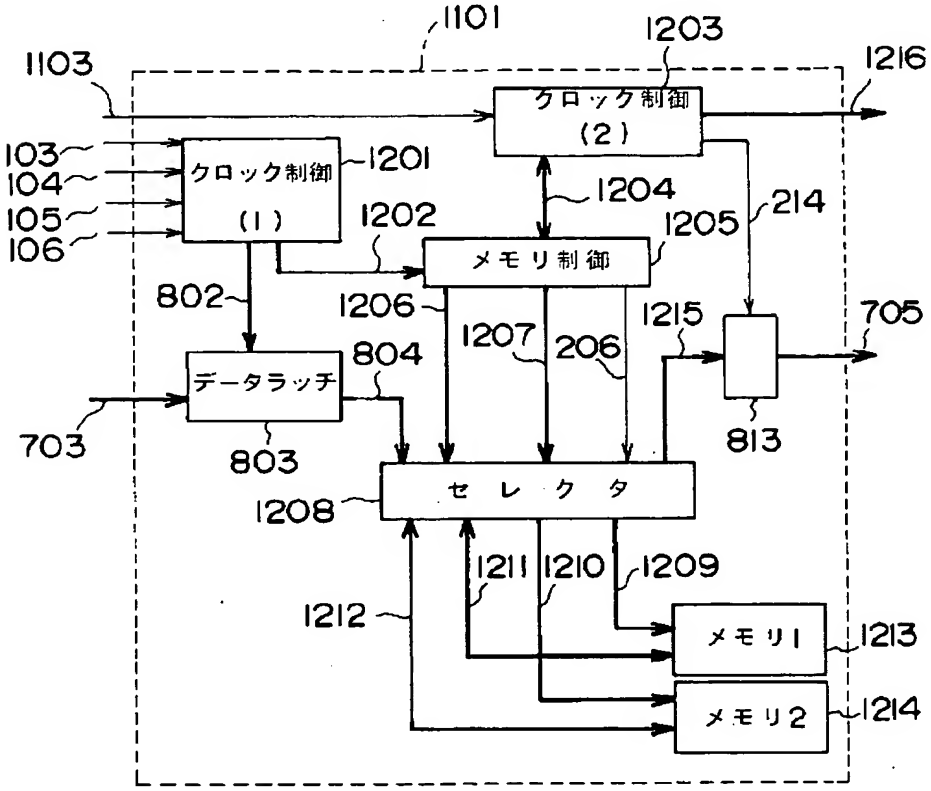
【図１１】

図11


109
127
111
113
108
115
704
103
カラム回路
104
S0
S1
S240
706
122
705
105
123
707
106
124
708
125
709
710
X0
X1
X2
X3
X4
X5
X6
X7
X957
X959
Y0
Y0
X956
X958
703
1103
1101
発振器
117
1102
Y239
Y239
112
116
701

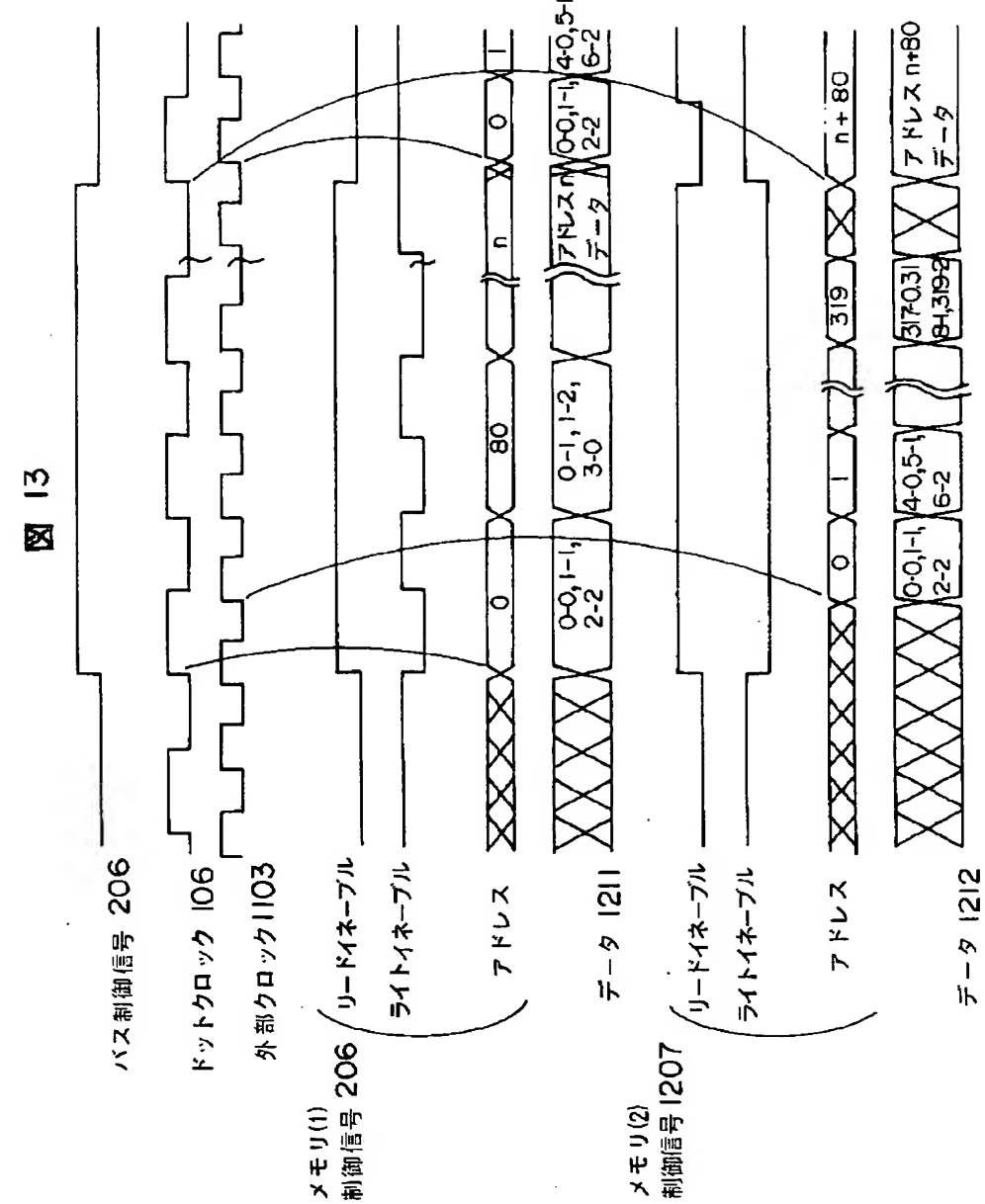
【図１２】

図 12


1101
1203
1103
1216
クロック制御
(2)
103
104
105
106
クロック制御
(1)
1201
1204
214
1202
1205
メモリ制御
802
1206
1207
206
1215
705
804
データラッチ
703
803
813
セレクタ
1208
1211
1210
1209
1212
メモリ1
1213
メモリ2
1214

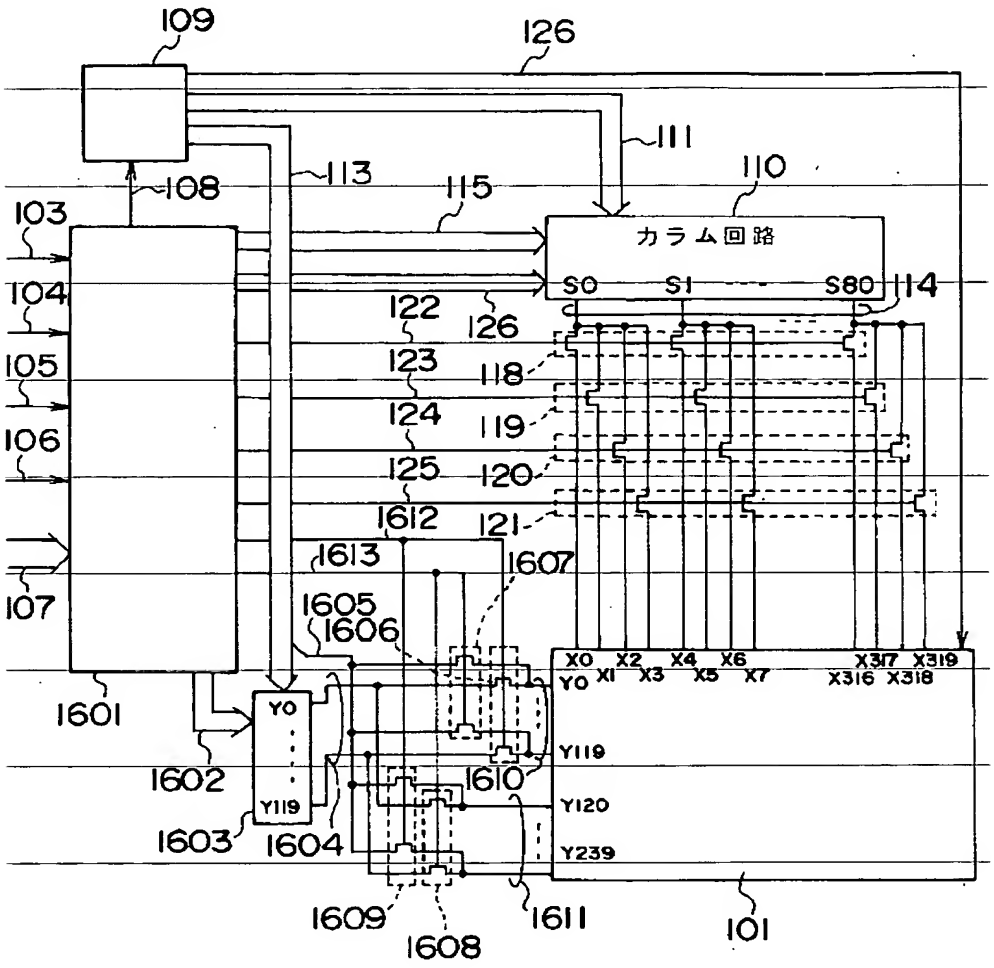
【図１３】

図 13


バス制御信号 206
ドットクロック 106
外部クロック1103
メモリ(1)
制御信号 206
リードイネーブル
ライトイネーブル
アドレス
0
n
80
1
データ 1211
0-0,1-1,
2-2
0-1,1-2,
3-0
アドレス n
データ
0-0,1-1,
2-2
4-0,5-1,
6-2
メモリ(2)
制御信号1207
リードイネーブル
ライトイネーブル
アドレス
0
1
319
n+80
データ 1212
0-0,1-1,
2-2
4-0,5-1,
6-2
317,0,31
84,319-2
アドレス n+80
データ

【図１５】

図 15


109
126
111
110
113
108
115
103
カラム回路
S0
S1
S80
114
104
122
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119
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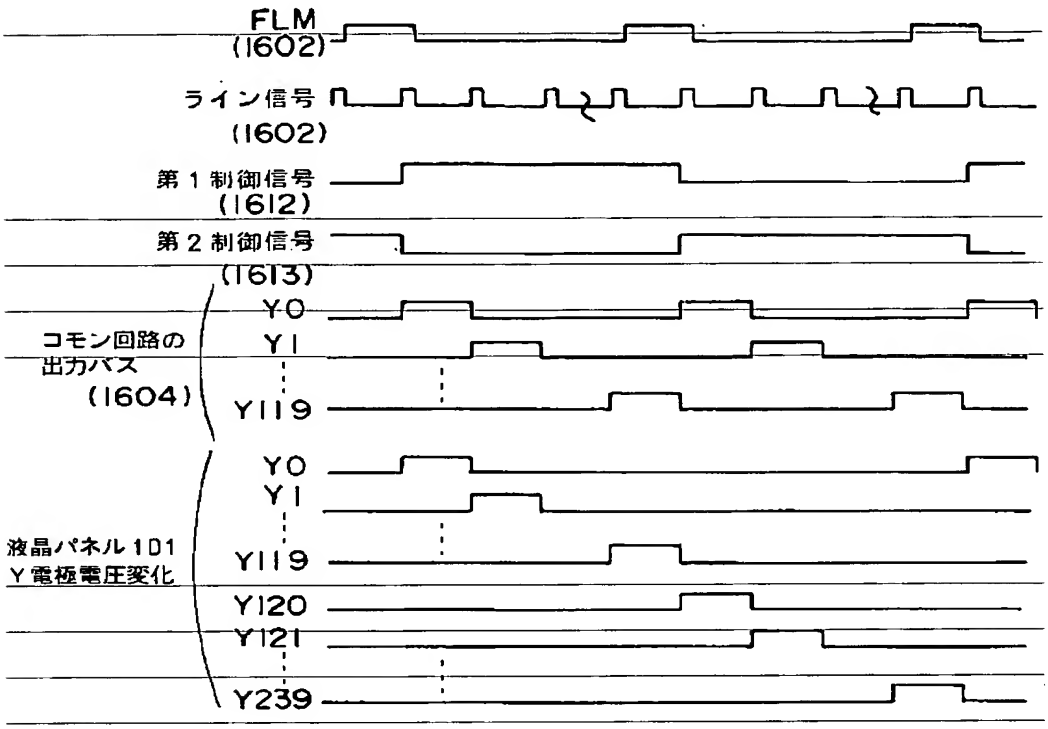
120
1612
121
1613
1607
107
1605
1606
X0
X2
X4
X6
X317
X319
Y0
X1
X3
X5
X7
X316
X318
1601
Y0
Y119
1602
1610
Y120
Y239
1603
1604
1609
1608
1611
101

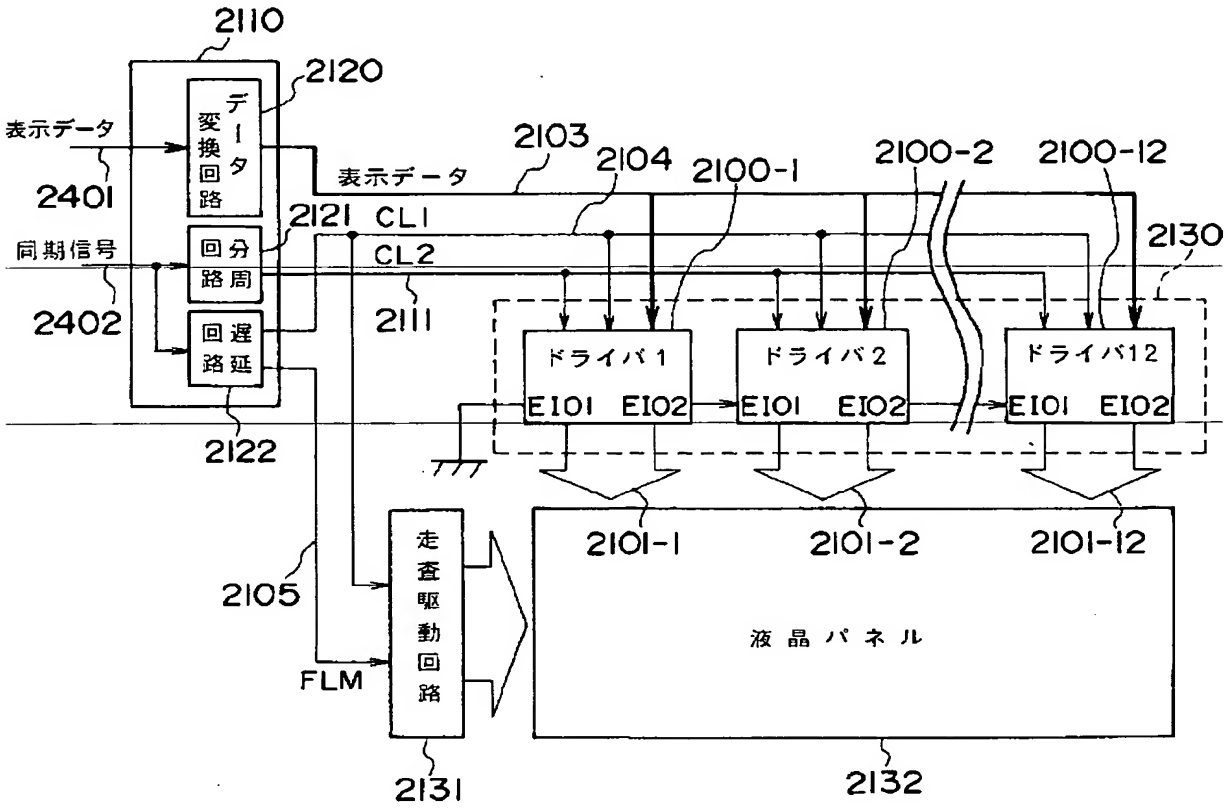
【図１６】

図 16


FLM
(1602)
ライン信号
(1602)
第１制御信号
(1612)
第２制御信号
(1613)
コモン回路の
出力パス
(1604)
Y0
Y1
Y119
液晶パネル101
Y電極電圧変化
Y0
Y1
Y119
Y120
Y121
Y239

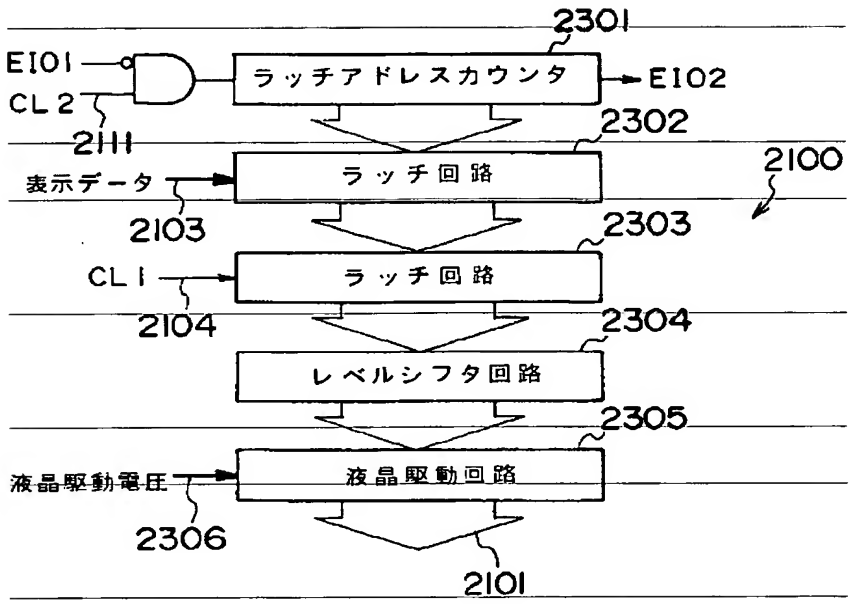
【図１７】

図 17


2110
2120
表示データ
2401
データ変換回路
2103
2104
2100-1
2100-2
2100-12
表示データ
2121
CL1
CL2
同期信号
2402
分周回路
遅延回路
2111
2130
ドライバ1
ドライバ2
ドライバ12
E101 E102
E101 E102
E101 E102
2122
2101-1
2101-2
2101-12
2105
走査駆動回路
液晶パネル
FLM
2131
2132

【図１９】

図 19



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G02F 1/133 550
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G02F 1/133 550
505
G09G 3/36

【手続補正書】
【提出日】平成１３年１月１１日（２００１．１．１１）
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正内容】
【特許請求の範囲】
【請求項１】　入力される表示データの表示を行う液晶表示装置であって、
複数のＸ電極と複数のＹ電極とを有する液晶パネルと、
階調電圧を生成し出力する電源回路と、
複数の出力端子を有し、前記液晶パネルの複数のＸ電極を駆動するカラム回路、および、Ｙ電極を選択駆動するコモン回路と、
表示データをカラム回路に出力すると共に、制御信号を出力して、カラム回路およびコモン回路を制御する表示コントローラと、
前記カラム回路の複数の出力電極と、前記液晶パネルの複数のＸ電極とを選択的に接続するスイッチ回路とを有し、
前記カラム回路は、前記表示コントローラから出力される表示データ、および、前記電源回路から出力される前記階調電圧が入力され、前記表示データに対応する前記階調電圧を前記複数の出力端子から出力し、
前記スイッチ回路は、前記カラム回路の複数の出力端子のそれぞれ毎に、前記各出力端子毎にグループ化された２以上のＸ電極のいずれかを選択的に前記対応する出力端子に接続するスイッチを有し、前記スイッチは、前記表示コントローラからの制御信号によりオンオフ制御されることを特徴とする液晶表示装置。
【請求項２】　請求項１に記載の液晶表示装置において、
前記スイッチ回路は、前記カラム回路の複数の出力端子のそれぞれ毎に、前記各出力端子毎にグループ化された２以上のＸ電極対応に配置された複数のスイッチを有し、前記複数のスイッチは、前記表示コントローラからに制御信号により選択的にオンオフ制御されることを特徴とする液晶表示装置。
【請求項３】　入力される表示データの表示を行う液晶表示装置であって、
複数のＸ電極と複数のＹ電極とを有する液晶パネルと、
複数の出力端子を有し、該複数の出力端子から前記表示データに対応して階調電圧を出力して、前記複数のＸ電極を駆動するカラム回路と、
前記液晶パネルの複数のＹ電極を駆動するコモン回路と、
前記階調電圧を生成し、前記カラム回路に出力する電源回路と、
２以上のグループに分類された前記複数のＸ電極のうち、選択された前記いずれかのグループに属する１以上のＸ電極を、前記カラム回路の前記階調電圧を前記表示データに対応して出力する出力端子に接続するＸ電極スイッチ回路と、
外部から入力される前記表示データを、それぞれ表示されるべき位置に対応するＸ電極が含まれる前記グループ毎に分けて、表示すべきグループの表示データを前記カラム回路へ出力する表示コントローラとを有し、
前記表示コントローラは、前記Ｘ電極スイッチ回路の複数のスイッチをオンオフ制御するスイッチ制御信号を前記Ｘ電極スイッチ回路に出力することを特徴とする液晶表示装置。
【請求項４】　請求項３記載の液晶表示装置であって、
前記表示コントローラは、

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少なくとも１ライン分のデータを記憶可能な第１のメモリと、
少なくとも１ライン分のデータを記憶可能な第２のメモリと、
外部から入力され表示データを取り入れ、前記第１のメモリおよび第２のメモリのうち書き込み対象として選択されたメモリに格納する書き込み手段と、
前記第１のメモリと前記第２のメモリのうち、前記書き込み手段による書き込み動作の対象となっていないメモリから、当該メモリに格納されている表示データを、対応するＸ電極の属する前記グループに含まれる表示データの集まり毎に、出力する読み出し手段と、
前記カラム回路が、任意のグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力を開始する前に、前記Ｘ電極スイッチ回路による前記グループの選択を、該次のグループのＸ電極と前記カラム回路の出力端子とが接続されるように変更させる選択指示手段と、
前記書き込み手段による前記表示データの書き込み動作の対象とされるメモリを、前記水平同期信号が有効になるのを契機として、前記第１のメモリと前記第２のメモリとの間で切り替えさせる制御手段とを有することを特徴とする液晶表示装置。

【請求項５】　請求４記載の液晶表示装置において、
前記表示コントローラは、外部からパラレルで入力された前記表示データを予め定められた画素数分受け付けて、前記受け付けた表示データを、当該表示データが対応するＸ電極の属するグループに基づいて分類して、各分類毎に出力する変換手段をさらに有し、
前記書き込み手段は、前記変換手段が出力する前記表示データを、前記第１のメモリおよび第２のメモリのうち書き込み対象として選択されたメモリに書き込むことを特徴とする液晶表示装置。

【請求項６】　請求項４記載の液晶表示装置において、
前記書き込み手段は、書き込みクロックに同期して書き込み動作を実行し、
前記読み出し手段は、前記書き込みクロックとは非同期の読み出しクロックに同期して、読み出し動作を実行し、
前記制御手段は、前記第１のメモリと前記第２のメモリの切り替えを、１画面分の表示データを書き込んだことを確認することで行うことを特徴とする液晶表示装置。

【請求項７】　請求項４～６のいずれか一項に記載の液晶表示装置において、
前記第１のメモリおよび前記第２のメモリは、当該メモリの記憶容量を変更可能に構成されていることを特徴とする液晶表示装置。

【請求項８】　請求項３に項記載の液晶表示装置において、
前記コモン回路は、

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出力端子を有し、選択された前記出力端子からは前記選択電圧を、他の出力端子からは非選択電圧を出力するコモン回路と、
前記Ｙ電極を１以上のグループに分け、いずれかのグループに属するＹ電極を前記コモン回路の前記出力端子と予め定められた対応関係で接続し、前記コモン回路と接続されていないＹ電極を前記電源回路の非選択電圧を出力する出力端子に接続するＹ電極スイッチ回路とを備えることを特徴とする液晶表示装置。

【請求項９】　複数のＸ電極と複数のＹ電極とを有する液晶パネルと、
複数の出力端子を有し、該複数の出力端子から前記表示データに対応して階調電圧を出力して、前記複数のＸ電極を駆動するカラム回路と、
前記液晶パネルの複数のＹ電極を駆動するコモン回路と、
前記階調電圧を生成し、前記カラム回路に出力する電源回路と、
２以上のグループに分類された前記複数のＸ電極のうち、選択された前記いずれかのグループに属する１以上のＸ電極を、前記カラム回路の前記階調電圧を前記表示データに対応して出力する出力端子に接続するＸ電極スイッチ回路とを備える液晶表示装置において用いられる表示コントローラであって、
少なくとも１ライン分のデータを記憶可能な第１のメモリと、
少なくとも１ライン分のデータを記憶可能な第２のメモリと、
外部から入力され表示データを取り入れ、前記第１のメモリおよび第２のメモリのうち書き込み対象として選択されたメモリに格納する書き込み手段と、
前記第１のメモリと前記第２のメモリのうち、前記書き込み手段による書き込み動作の対象となっていないメモリから、当該メモリに格納されている表示データを、対応するＸ電極の属する前記グループに含まれる表示データの集まり毎に、出力する読み出し手段と、
前記カラム回路が、任意のグループに属するＸ電極に階調電圧を出力し終わった後、次のグループのＸ電極に対応する階調電圧の出力を開始する前に、前記Ｘ電極スイッチ回路による前記グループの選択を、該次のグループのＸ電極と前記カラム回路の出力端子とが接続されるように変更させる選択指示手段と、
前記書き込み手段による前記表示データの書き込み動作の対象とされるメモリを、前記水平同期信号が有効になるのを契機として、前記第１のメモリと前記第２のメモリとの間で切り替えさせる制御手段とを有することを特徴とする表示コントローラ。

【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】０００１

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【補正方法】変更
【補正内容】
【０００１】
【産業上の利用分野】本発明は、パソコン、ワークステーション等の表示データを液晶パネルに表示させるのに好適な液晶表示コントローラ、および、液晶表示装置に関する。
【手続補正３】
【補正対象書類名】明細書
【補正対象項目名】００２８
【補正方法】変更
【補正内容】
【００２８】本発明は、従来の液晶駆動回路を用いつつ、画素ピッチを微細化した液晶パネルに対応可能な表示コントローラ、および、液晶表示装置を提供することを目的とする。
【手続補正４】
【補正対象書類名】明細書
【補正対象項目名】００４５
【補正方法】変更
【補正内容】
【００４５】本実施例の液晶表示装置は、図１に示すとおり、液晶パネル１０１と、液晶パネル１０１のＸ電極を駆動するためのカラム回路１１０と、液晶パネル１０１のＹ電極を駆動するためのコモン回路１１２と、外部から入力されてくる各種信号および表示データ等に従って、カラム回路１１０及びコモン回路１１２を作動させる表示コントローラ１０２と、電源回路１０９と、から構成されている。当然、これらは、各種信号等を授受するための信号線１０３，１０４，１０５，１０６，１０８，１２７，１２２～１２５、およびバス１１１，１１３，１１５，１２６，１１７，１０７によって接続されている。さらに、本実施例では、液晶パネル１０１とカラム回路１１０との接続を、表示コントローラ１０２からの指示に従って作動するスイッチ群１１８～１２１を介して行っている。本実施例は、このスイッチ群１１８～１２１を設けたこと、及び、これに対応した表示制御を最大の特徴とするものである。
【手続補正５】
【補正対象書類名】明細書
【補正対象項目名】００６７
【補正方法】削除
【手続補正６】
【補正対象書類名】明細書
【補正対象項目名】００６８
【補正方法】削除
【手続補正７】
【補正対象書類名】明細書
【補正対象項目名】００８０
【補正方法】変更

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【補正内容】
【００８０】読み出しクロックを８０個出力した後、クロック制御部２０１は、カラム制御信号１１５に含まれている、出力クロックを”有効”にする。なお、この出力クロックは、階調電圧を出力するタイミングをカラム回路１１０へ指示するためのものである。また、これと並行して、クロック制御部２０１は、スイッチ制御信号１２２～１２５によって、その時、表示データ１２６として出力しているデータの対応するスイッチ群をＯＮに、また、他のスイッチ群はＯＦＦにする。例えば、その時の表示データ１２６が、第１スイッチ群１１８に対応したもの（図５においては、アドレス８０～１５９）であれば、第１スイッチ群１１８をＯＮに、第２、第３、第４スイッチ群１１９，１２０，１２１をＯＦＦにする。これにより、カラム回路１１０は、その時の表示データ信号１２６に対応した階調電圧を、次の出力クロックが有効になるまでの期間、所定のＸ電極にのみ出力することになる。なお、スイッチ制御信号１２２～１２５の出力のタイミングは、カラム回路１１０が、前の表示データに対応する階調電圧を出力し終わってから、次の表示データの階調電圧の出力を開始するまでであれば、特に限定されない。場合によっては、目的とする表示データの階調電圧の出力を開始した後であっても、構わない。適宜、実際の各部回路の特性等にあわせて設定すれば良い。
【手続補正８】
【補正対象書類名】明細書
【補正対象項目名】００８６
【補正方法】変更
【補正内容】
【００８６】ライン信号が次回有効になると、コモン回路１１２は今度は電極ｙ１に選択電圧を出力する。電極ｙ０および電極ｙ２～ｙ２３９には非選択電圧を出力する。これにより、その時Ｘ電極に印加されている階調電圧は、電極ｙ１に対応する行の画素にだけ印加される。この動作を電極ｙ２３９まで繰り返すことで、１画面分の表示が完了する。この後、表示コントローラ１０２は、ＦＬＭを有効にして、再び電極ｙ０から順次選択電圧を出力してゆく。
【手続補正９】
【補正対象書類名】明細書
【補正対象項目名】０１００
【補正方法】変更
【補正内容】
【０１００】データラッチ回路８０３は、３画素分づつパラレルで入力されてくる表示データ７０３を、スイッチ群７０７～７１０に対応して並び換えるためのものである。該データラッチ回路８０３は、並び変えた後の表示データを出力バス８０４から出力している。データラッチ回路８０３については、この後図９を用いてさらに

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詳細に説明する。本実施例では、データラッチ回路８０３は、表示データの並びを変換する変換手段として機能する。

【手続補正１０】

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【補正対象書類名】明細書

【補正対象項目名】０１６７

【補正方法】削除